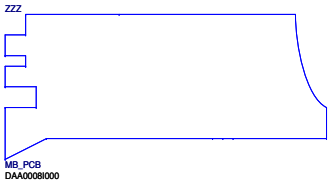
MODEL NAME : *ZAZ00*
PCB NO : *LA-B441P*
BOM P/N : *TBD*



Dell/Compal Confidential

Schematic Document

Dino (Broadwell ULT)

2014-10-16

Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

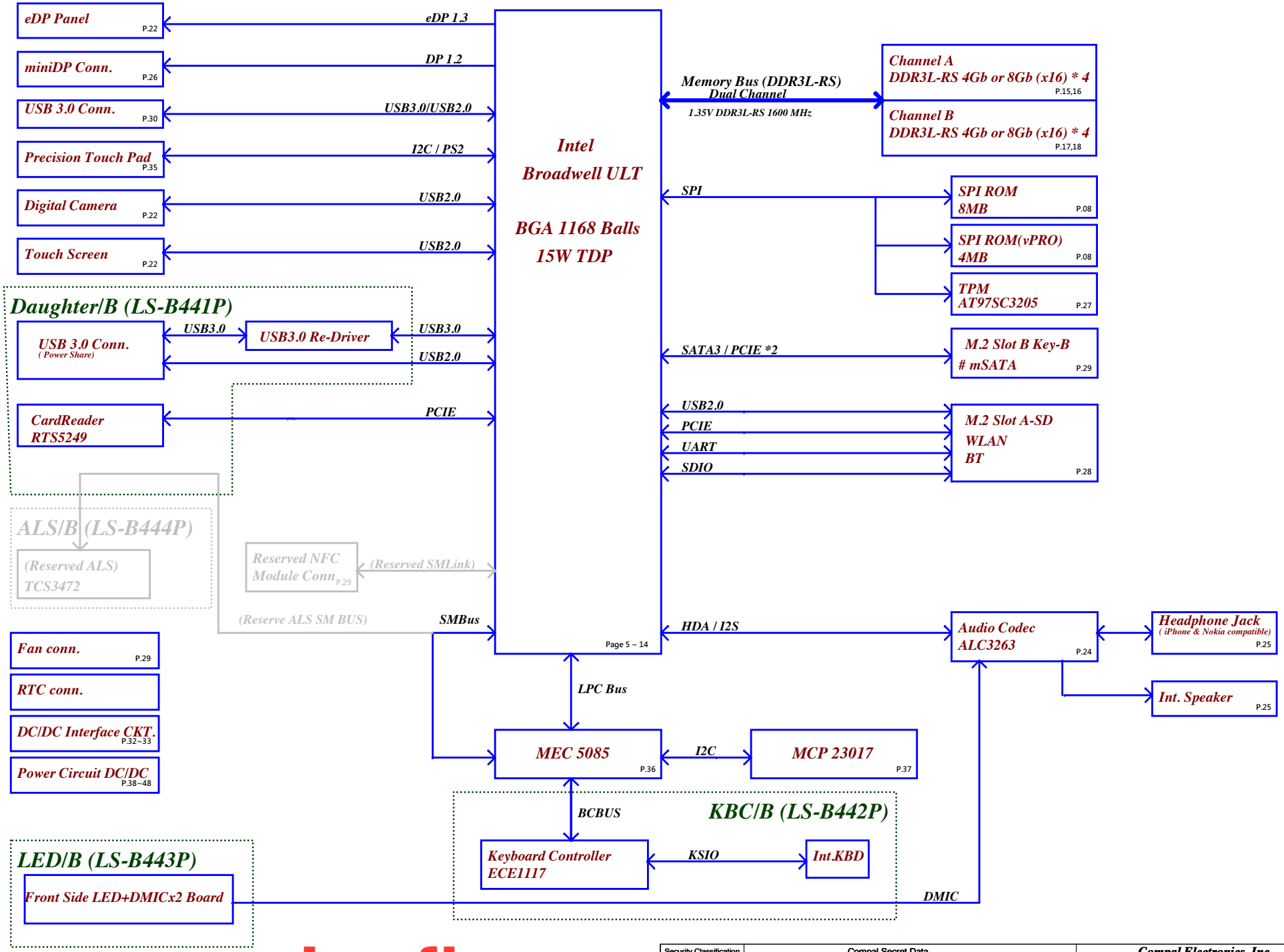
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: *P01-Cover Page*

Size	Document Number	Rev
	LA-B441P	1.0

Date: Thursday, October 16, 2014 Sheet 1 of 50



www.vinafix.vn

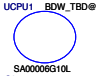
Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title	P02-Block Diagram		
Size	Document Number	LA-B441P	Rev 1.0
Date: Saturday, October 04, 2014	Sheet 2 of 50		

CPU Option

UCPU1 BDW_TBD@



SA00006G10L
CL8064701325204 QDJ9

DRAM Option

Micron 4G	UD28 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD29 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD31 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD32 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD1 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD7 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD3 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E	UD4 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E
Micron 8G	UD28 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD29 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD31 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD32 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD1 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD7 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD3 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E	UD4 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E
Hynix 4G	UD28 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD29 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD31 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD32 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD1 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD7 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD3 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR	UD4 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR
Hynix 8G	UD28 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD29 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD31 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD32 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD1 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD7 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD3 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR	UD4 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR
Elpida 4G	UD28 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD29 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD31 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD32 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD1 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD7 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD3 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0	UD4 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0
Elpida 8G	UD28 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD29 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD31 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD32 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD1 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD7 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD3 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0	UD4 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0

DRAM Config Option

MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
RH314 Micron_4G@ SD028100280 10K_0402_5%~D	RH315 Micron_4G@ SD028100280 10K_0402_5%~D	RH316 Micron_4G@ SD028100280 10K_0402_5%~D
RH314 Micron_8G@ SD028100280 10K_0402_5%~D	RH315 Micron_8G@ SD028100280 10K_0402_5%~D	RH303 Micron_8G@ SD028100280 10K_0402_5%~D
RH314 Hynix_4G@ SD028100280 10K_0402_5%~D	RH180 Hynix_4G@ SD028100280 10K_0402_5%~D	RH316 Hynix_4G@ SD028100280 10K_0402_5%~D
RH314 Hynix_8G@ SD028100280 10K_0402_5%~D	RH180 Hynix_8G@ SD028100280 10K_0402_5%~D	RH303 Hynix_8G@ SD028100280 10K_0402_5%~D
RH271 Elpida_4G@ SD028100280 10K_0402_5%~D	RH315 Elpida_4G@ SD028100280 10K_0402_5%~D	RH316 Elpida_4G@ SD028100280 10K_0402_5%~D
RH271 Elpida_8G@ SD028100280 10K_0402_5%~D	RH315 Elpida_8G@ SD028100280 10K_0402_5%~D	RH303 Elpida_8G@ SD028100280 10K_0402_5%~D

LA-B441P

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date 2013/10/28	Title: P03-BoM Option
			Size / Document Number / Rev 1.0
			Date: Saturday, October 04, 2014 Sheet 3 of 50

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Board ID Table for AD channel

RE79	CE54	REV
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3(On IOB)
	1	External USB3(On MB)
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	
	6	
	7	

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	mini-DP
	2	

SMBUS Control Table

Reserve ALS SMBUS

	SOURCE	BATTERY	ALS	Charger	NFC	XDP	Touch Pad
I2C1C_CLK I2C1C_DATA	MEC5085	V					
I2C1D_CLK I2C1D_DATA	MEC5085						
I2C1G_CLK I2C1G_DATA	MEC5085		V	V			
PCH_SML0CLK PCH_SML0DATA	PCH				V		
PCH_SML1CLK PCH_SML1DATA	PCH						
SMBCLK SMBDATA	PCH					V	
I2C1_CLK I2C1_DATA	PCH						V

Link

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Card Reader	Lane 1	Card Reader
	CLKOUT_PCIE1		Lane 2	
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	NGFF CARD WLAN	Lane 4	NGFF CARD WLAN
	CLKOUT_PCIE4		Lane 5	
	CLKOUT_PCIE5	mSATA/ PCIe	Lane 6	mSATA/ PCIe(Port0+Port1)
	FLEX CLK#	DESTINATION		
	CLKOUT_LPC_0	EC LPC		
	CLKOUT_LPC_1	TPM		

SATA PORT#	DESTINATION
SATA0	
SATA1	
SATA2	
SATA3	m-SATA

Symbol Note :

: means Digital Ground

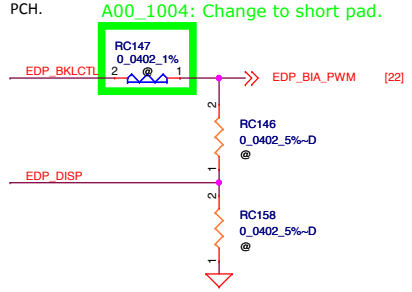
: means Analog Ground

Security Classification: Compal Secret Data
Issued Date: 2013/07/04 Deciphered Date: 2013/10/28
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

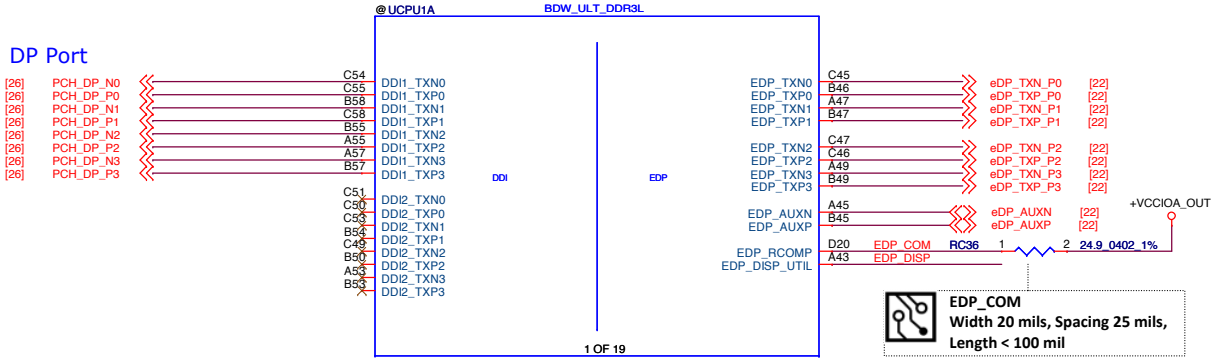
Compal Electronics, Inc.
Title: P04-Notes List
Size: Document Number: LA-B441P Rev: 1.0
Date: Saturday, October 04, 2014 Sheet 4 of 50

Low voltage multipurpose DISP_UTIL pin on the processor for backlight modulation control of embedded panels and S3D device control for active shutter glasses. This pin will co-exist with functionality similar to existing BKLTCTL pin on the PCH.

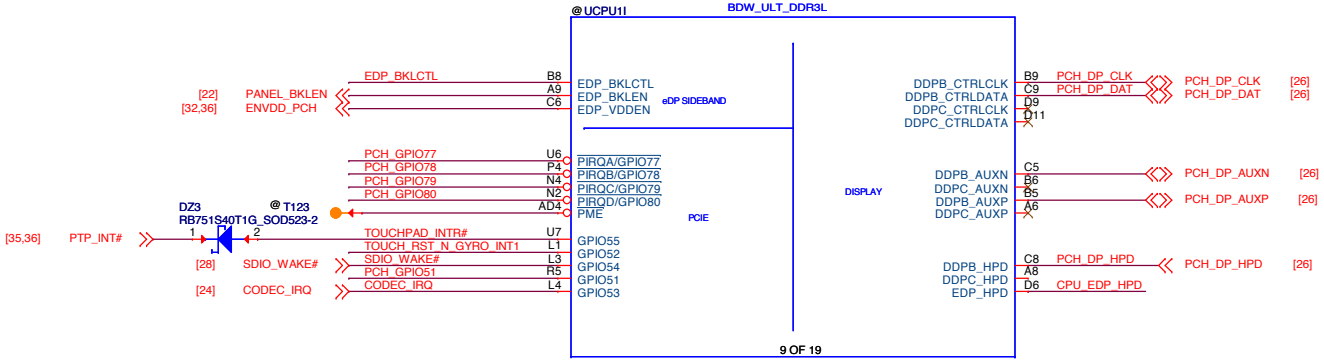
A00_1004: Change to short pad.

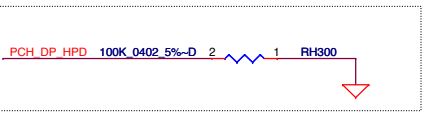


DP Port

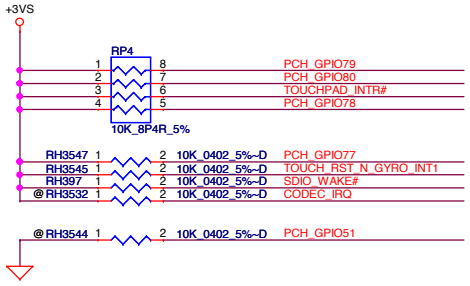


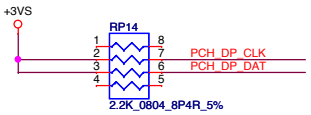
EDP_COM
Width 20 mils, Spacing 25 mils, Length < 100 mil





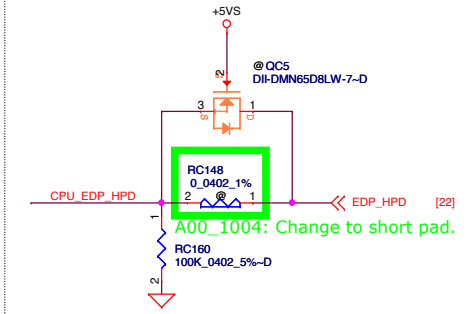
GPIO Signals





Functional Strap Definitions	
DDI Port 1 Disabling	
DDPB_CTRLDATA	Enable : Pull up to 3.3V with 2.2K+-5% ohm Disable : No connect

Functional Strap Definitions	
DDI Port 2 Disabling	
DDPC_CTRLDATA	Enable : Pull up to 3.3V with 2.2K+-5% ohm Disable : No connect



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Title	P05-MCP(1/10) DDI,EDP
Size	Document Number: LA-B441P
Rev	1.0
Date:	Sunday, October 05, 2014
Sheet	5 of 50

H_PECI
1. Total Length : 15 inchs
2. Resistor Value (±5%) : 43 ohm
3. Breakin/Breakout Length Max :0.4 ~ 1 inchs

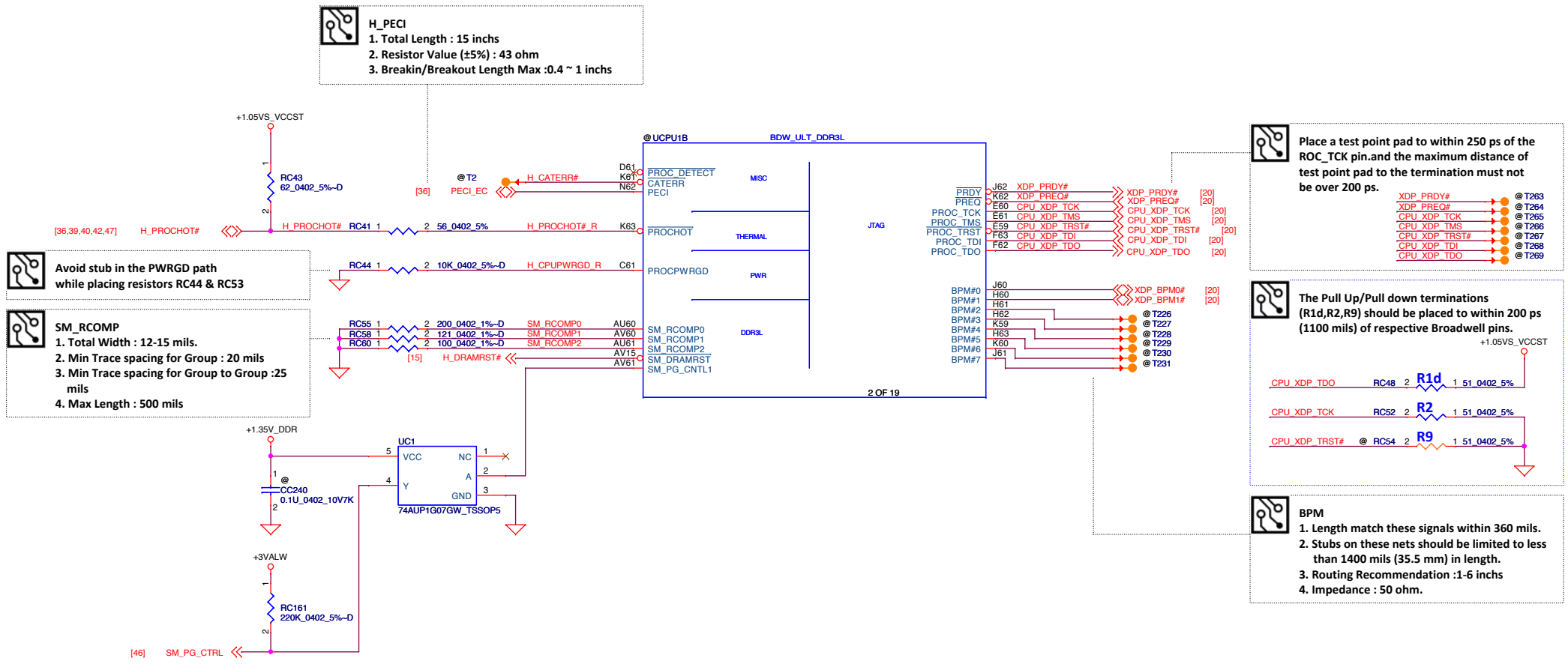
Avoid stub in the PWRGD path while placing resistors RC44 & RC53

SM_RCOMP
1. Total Width : 12-15 mils.
2. Min Trace spacing for Group : 20 mils
3. Min Trace spacing for Group to Group :25 mils
4. Max Length : 500 mils

Place a test point pad to within 250 ps of the ROC_TCK pin.and the maximum distance of test point pad to the termination must not be over 200 ps.

The Pull Up/Pull down terminations (R1d,R2,R9) should be placed to within 200 ps (1100 mils) of respective Broadwell pins.

BPM
1. Length match these signals within 360 mils.
2. Stubs on these nets should be limited to less than 1400 mils (35.5 mm) in length.
3. Routing Recommendation :1-6 inchs
4. Impedance : 50 ohm.



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

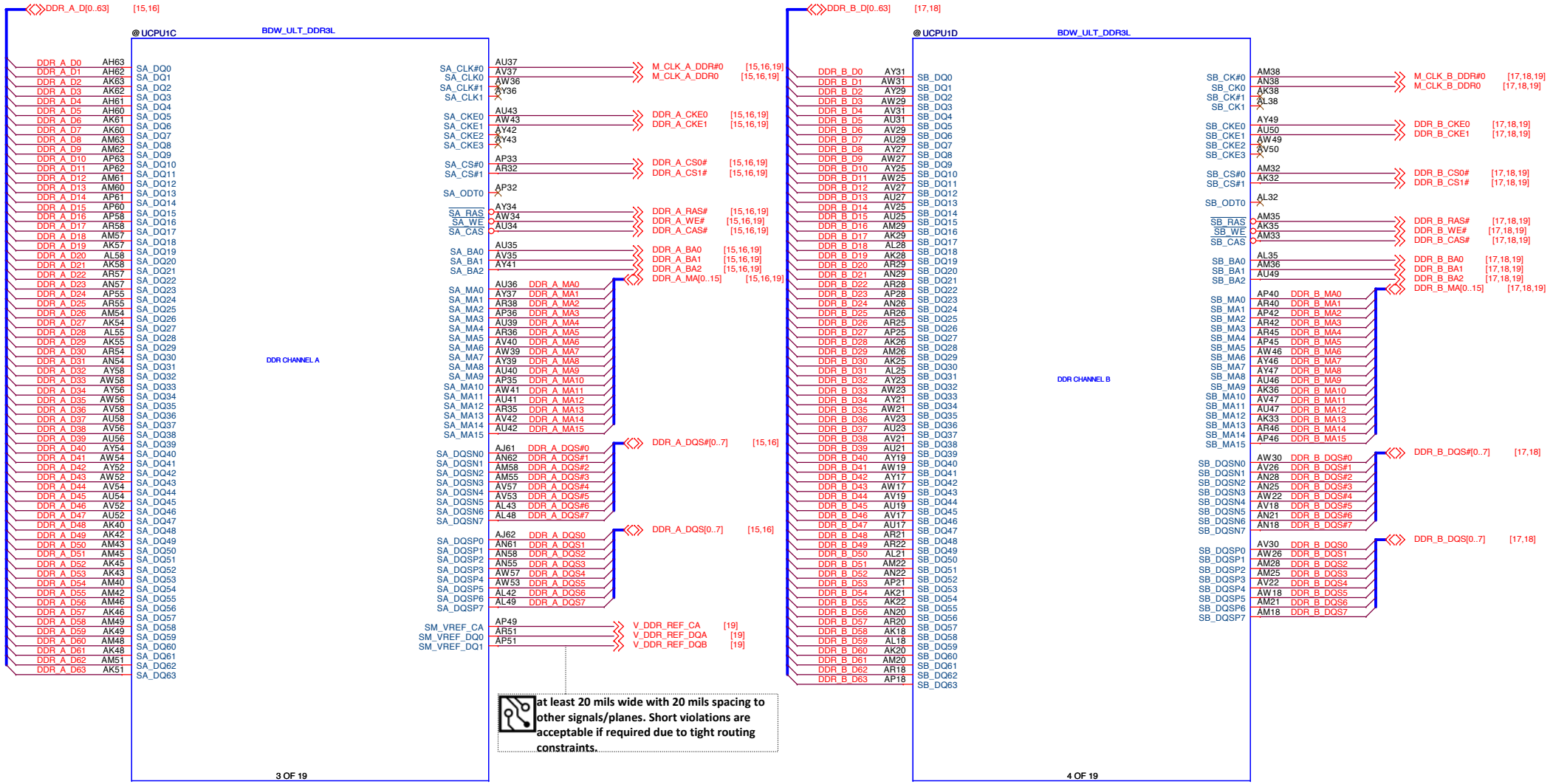
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P06-MCP(2/10) PM,XDP

Size | Document Number: LA-B441P | Rev: 1.0

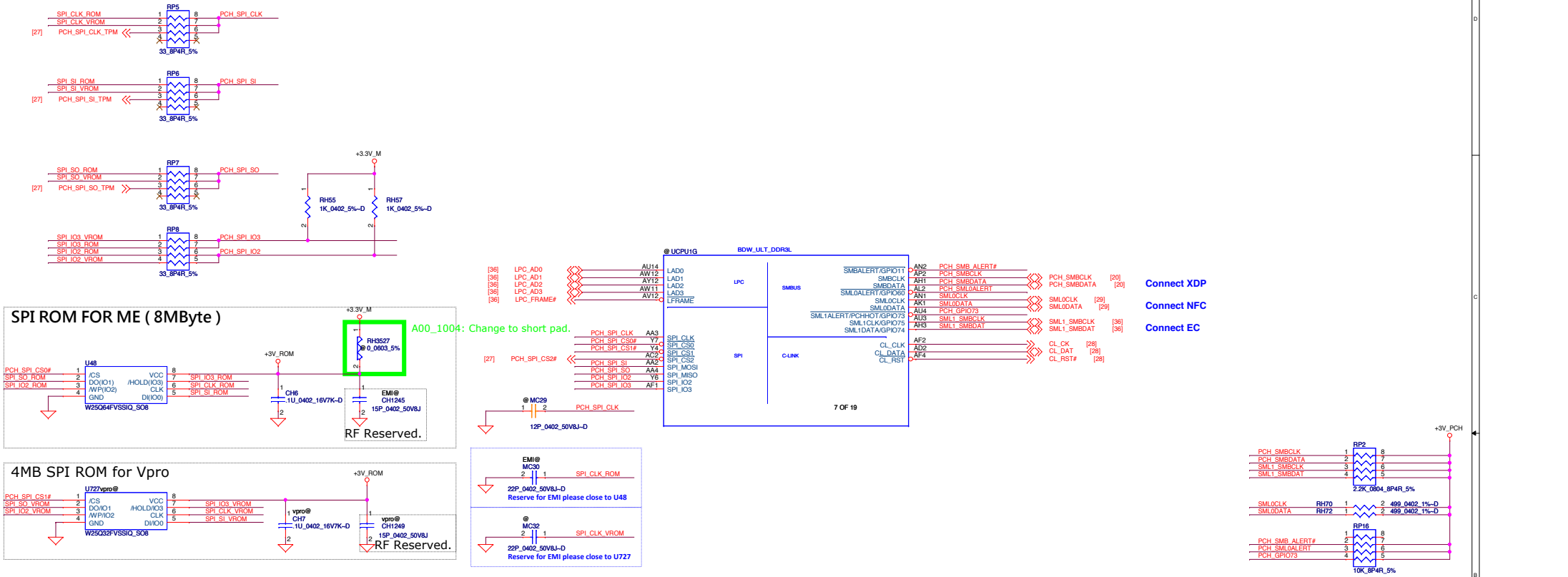
Date: Saturday, October 04, 2014 | Sheet 6 of 50



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	P07-MCP(3/10) DDRIII		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Saturday, October 04, 2014	Sheet 7 of 50	



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

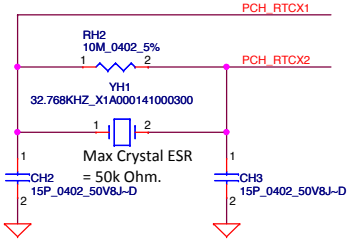
Compal Electronics, Inc.

Title: P08-MCP(4/10) LPC,SPI,SMBUS,CL

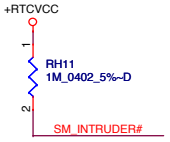
Size	Document Number	Rev
	LA-B441P	1.0

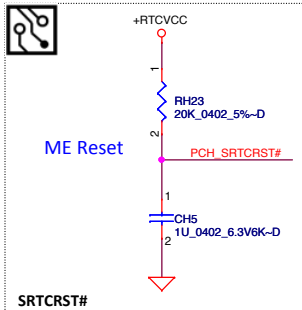
Date: Sunday, October 05, 2014 Sheet 8 of 50

RTCX1 RTCX2
1. Total Length : 1000 mils
2. Space > 15 mils
3. Resistor Value (±5%) : 10M

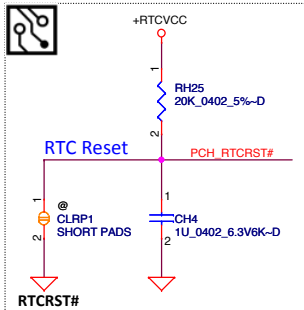


INTRUDER#
1. Critical Low Speed Signal
2. Space > 15 mils
3. Frequency to Avoid 32K
4. All critical signals must stay away from potential glitch or noise sources on the platform.





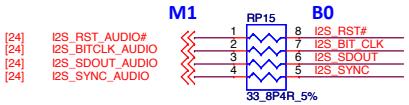
SRTCRST#
1. Total Length : 8000 mils
2. Space > 15 mils
3. Impedance Target 50 Ω ±15% for Microstrip.
4. RC time delay between 18 ms - 25 ms must be met.
5. There must not be a jumper for SRTCRST# pin.

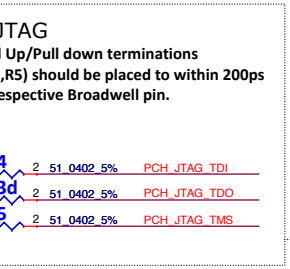


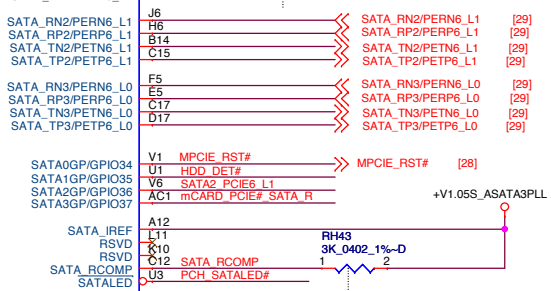
RTCRST#
1. Total Length : 8000 mils
2. Space > 15 mils
3. Impedance Target 50 Ω ±15% for Microstrip.
4. RC time delay between 18 ms - 25 ms must be met.

1.When SATA and PCIe are muxed, always route according to SATA design guidelines.
2. Breakout < 600 mils
3. Zdiff : 85 ohm
4. Isolation to Other Signal Groups: Breakout : 8 mils/ Main routing : 20 mils in MS, 15 mils in SL,DSL
5. Max Length : 2 via Max 8", 3 vias Max 7"
6. Within Layer Max Mismatch : 15 mils.
7. Total Length Max Mismatch : 10 mils.
8. AC capacitors to be placed as close as possible to the connector. Maximum distance from AC capacitors to connector is 500 mils.
9. Minimum breakout pair-to-pair spacing of 3.5 mils is allowed for a maximum length of 20 mils within the 600 mils breakout.
10. Design constraint: breakout routing should be non-interleaved to mitigate concerns on near-end crosstalk.

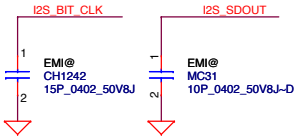
HDA_SDIN/HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST#
1. BO < 500 mils
2. 1000 mils < M1 < 14000 mils.
3. Trace Length Matching (HDA_SDIO,HDA_BCLK,HDA_SDOUT)
4. Resistor Value : 33 ohm





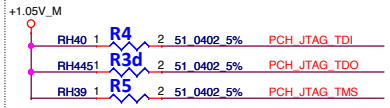


RF Reserved.

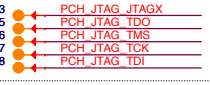


PCH JTAG

The Pull Up/Pull down terminations (R4,R3d,R5) should be placed to within 200ps of the respective Broadwell pin.

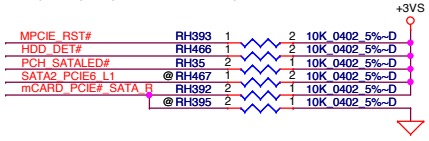


TP should be placed to with 250ps (1380 mils) of the respetive Haswell ULT pins, and the distance between TP and termination (if any) must be within 200ps (1100 mils).



GPIO Signals

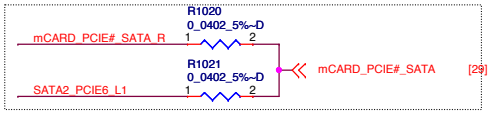
SATA0GP,SATA1GP,SATA2GP,SATA3GP
1. Needs a weak pull-up:10 KΩ ±10% pull-up to V3.3.
2. Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2–10 KΩ on the motherboard. Either pull-up or pull-down is acceptable.

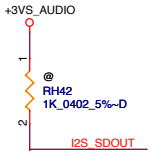


SATA_RCOMP, SATA_IREF
1. Break-out : 4 mils
2. 12-15 mil trace with <0.2 Ω.
3. Length total <= 500 mils.
4. Requires 12 mils isolation from all High Speed I/O and clocks.

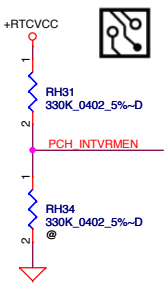
SATA_RCOMP
1. Tied up to a clean 1.05V source (VCCASATA3PLL) with no capacitor on the net.
2. 3 KΩ ±1% precision pull-up resistor

SATA_IREF
1. Pull-up direct to 1.05V (VCCASATA3PLL).





Functional Strap Definitions	
Flash Descriptor Security Override	
HDA_SDO/ I2S0_TXD	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

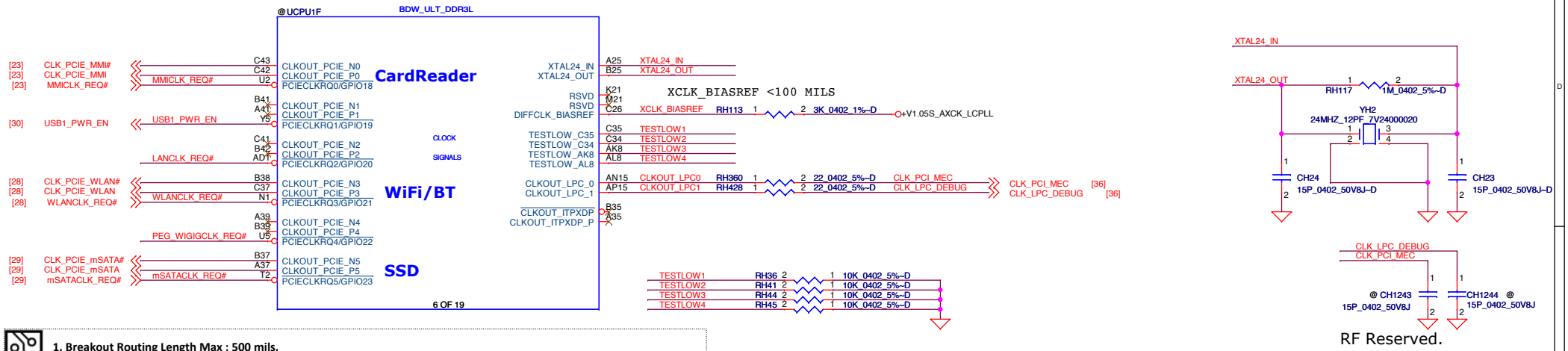


INTRUDER#
1. Critical Low Speed Signal
2. Space > 15 mils
3. Frequency to Avoid 32K
4. All critical signals must stay away from potential glitch or noise sources on the platform.

Functional Strap Definitions	
Integrated VRM	
INTVRMEN	0 = DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 are powered from an external power source (should be connected to an external VRM). 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28
Title	P09-MCP(4/10) RTC,AUDIO,SATA		
Size	Document Number LA-B444P		Rev 1.0
Date: Saturday, October 04, 2014		Sheet 9 of 50	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



1. Breakout Routing Length Max : 500 mils.
2. Breakin Routing Length Max : 1500 mils
3. Routing Min and Max Length : 2"~9"
4. Differential Pair Length Matching. <25 mils for PCIe, <20 mils for ITP
6. Max Vias : 4
5. Stitching vias should be placed with this spacing:
   a).30-mils pitch between differential clock via and closest stitching GND-via.
   b). Every differential clock via must have at least one GND stitching via with a maximum spacing of 30 mils (0.762 mm).
6. Placement of additional stitching vias, where possible, is recommended.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28
Title	P10-MCP(5/10) CLOCKS		
Size	Document Number LA-B444P		Rev 1.0
Date: Saturday, October 04, 2014	Sheet 10 of 50		

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Deep S3 (Pop RH430)

Deep S3 support, connect to EC

NON-Deep S3 Support

A00_1004: Change to short pad.

Deep S3 support, connect to DSW power rail

PCH Strap PIN

DSWODVREN - On Die DSW VR Enable
* H : Enable
L : Disable

closed MCP 2000 mils

TLS Confidentiality

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
*High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Deep S3 Support

Reserve for RF please close to UH1

GPIO86 have internal pull down

Boot BIOS Strap

PCH_GPIO86	Boot BIOS Location
* 0	SPI

GPIO66 have internal pull down

A16 SWAP OVERRIDE STRAP	
STP_A16OVR	*LOW = A16 SWAP OVERRIDE HIGH = NO OVERRIDE

I2C is daisy chain routing with pull up on the last device

Width = 15 mil, Spacing = 12 mil
Close PCH within 500 mil

DDR Memory Configuratino Type Strap pin

GPIO Pin	Pin Name	Micron 4G SA00005TH0L	TBD	Hynix 4G SA00006JF0L	Hynix 8G SA00006Q90L	TBD	Elpida 8G SA00006090L
PCH_GPIO70	MEM_CONFIG0	0	1	0	1	0	1
PCH_GPIO93	MEM_CONFIG1	0	0	1	1	0	0
PCH_GPIO94	MEM_CONFIG2	0	0	0	0	1	1

RF Reserved.

*LOW=Default
HIGH=No Reboot

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

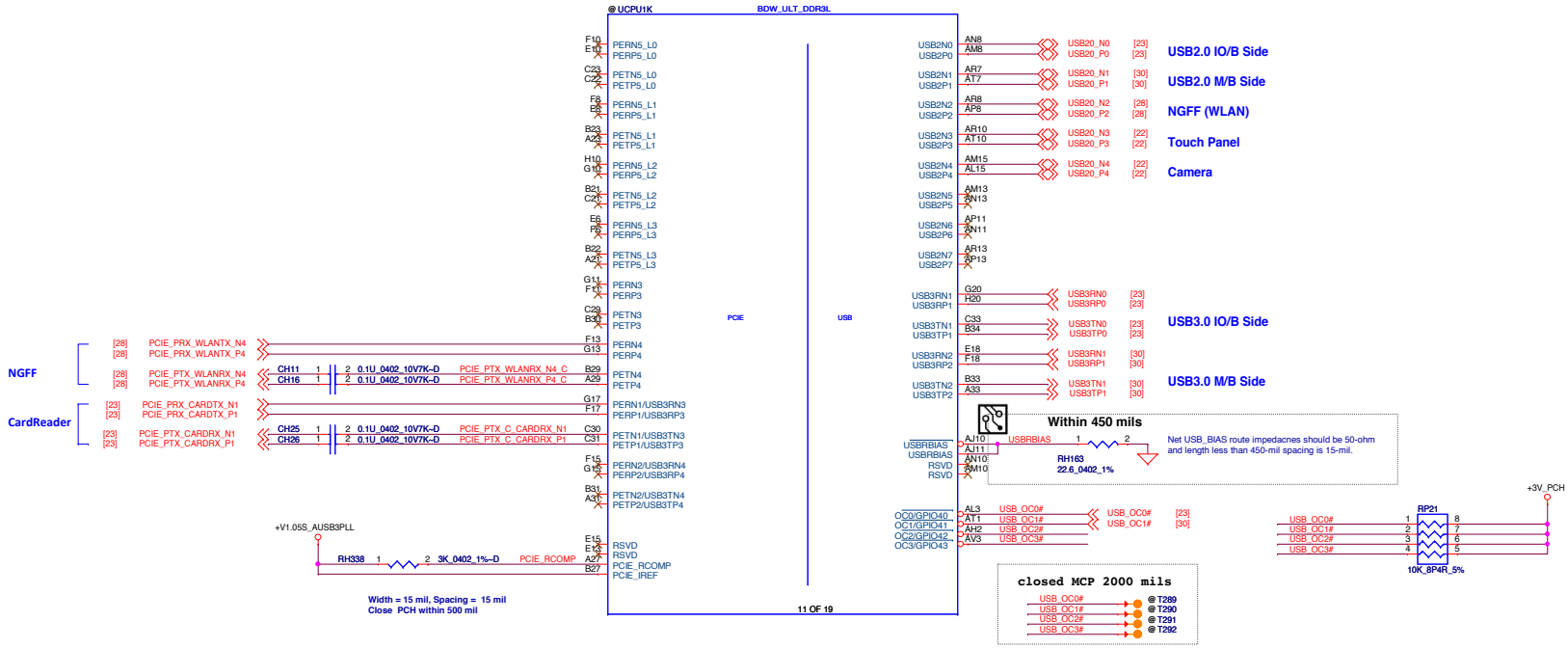
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

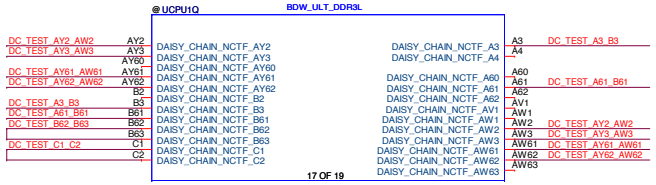
Compal Electronics, Inc.

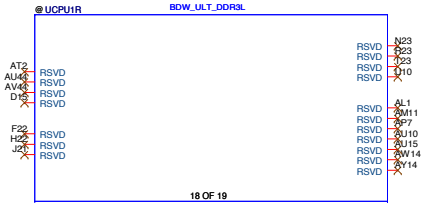
Title: P11-MCP(7/10) PM,GPIO,LPIO,MISC

Size: | Document Number: LA-B441P | Rev: 1.0

Date: Sunday, October 05, 2014 | Sheet 11 of 50



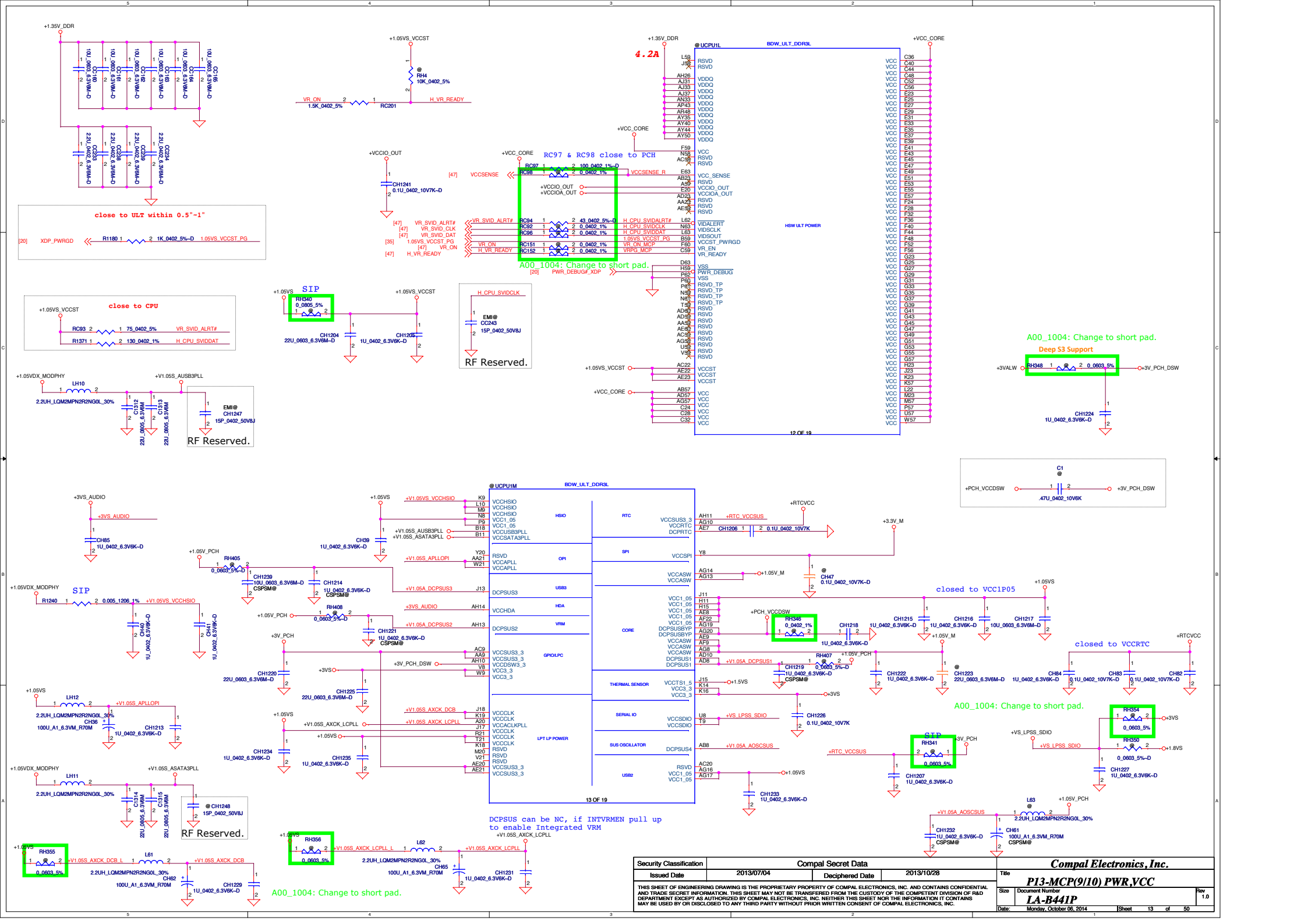




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	P12-MCP(8/10) PCIE,USB		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Saturday, October 04, 2014	Sheet	12 of 50


+1.35V_DDR
+1.05VS_VCCST
+VCC_CORE
+VCCIO_OUT
4.2A
@ UCPU1L
BDW_ULT_DDR3L
HSW ULT POWER
12 OF 19
RC97 & RC98 close to PCH
close to ULT within 0.5"~1"
close to CPU
A00_1004: Change to short pad.
Deep S3 Support
SIP
RF Reserved.
@ UCPU1M
13 OF 19
closed to VCC1P05
closed to VCCRTC
DCPSUS can be NC, if INTVRMEN pull up
to enable Integrated VRM
Security Classification
Compal Secret Data
Issued Date
2013/07/04
Deciphered Date
2013/10/28
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
P13-MCP(9/10) PWR,VCC
Size
Document Number
LA-B441P
Rev
1.0
Date: Monday, October 06, 2014
Sheet 13 of 50

Place a test point pad to within 250 ps of the ROC_TCK pin.and the maximum distance of test point pad to the termination must not be over 200 ps.

@T293 CFG3

2 1 CFG4
1K_0402_1%~D RC81

eDP Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

8.2K_0402_1% 2 1 RC155 TD_IREF
49.9_0402_1%~D 2 1 RC153 CFG_RCOMP
49.9_0402_1%~D 2 1 RC154 PROC_OPI_COMP

Width = 15 mil, Spacing = 15 mil
Close PCH within 500 mil

@UCPU1S BDW_ULT_DDR3L

[20] CFG0 AC60 CFG0
[20] CFG1 AC62 CFG1
[20] CFG2 AC63 CFG2
[20] CFG3 CFG3 AA63 CFG3
[20] CFG4 CFG4 AA60 CFG4
[20] CFG5 Y62 CFG5
[20] CFG6 Y61 CFG6
[20] CFG7 Y60 CFG7
[20] CFG8 V62 CFG8
[20] CFG9 V61 CFG9
[20] CFG10 V60 CFG10
[20] CFG11 U60 CFG11
[20] CFG12 T63 CFG12
[20] CFG13 T62 CFG13
[20] CFG14 T61 CFG14
[20] CFG15 T60 CFG15

[20] CFG16 AA62 CFG16
[20] CFG18 U63 CFG18
[20] CFG17 AA61 CFG17
[20] CFG19 U62 CFG19

CFG_RCOMP V63 CFG_RCOMP
A5 RSVD
E1 RSVD
D1 RSVD
J20 RSVD
H19 RSVD
TD_IREF B12 TD_IREF

RESERVED

RSVD_TP AV63
RSVD_TP AU63
RSVD_TP C63
RSVD_TP C62
RSVD B43
RSVD_TP A51
RSVD_TP B51
RSVD_TP L60
RSVD N60
RSVD W23
RSVD Y22
RSVD AY15 PROC_OPI_COMP
PROC_OPI_RCOMP
RSVD AV62
RSVD D58
VSS P22
VSS N21
RSVD P20
RSVD R20

19 OF 19

@UCPU1N BDW_ULT_DDR3L

A11 A14 A18 A24 A28 A32 A36 A40 A44 A48 A52 A56 AA1 AA58 AB10 AB20 AB22 AB7 AC61 AD21 AD3 AD63 AE10 AE5 AE58 AF11 AF12 AF14 AF15 AF17 AF18 AG1 AG11 AG21 AG23 AG60 AG61 AG62 AG63 AH17 AH19 AH20 AH22 AH24 AH28 AH30 AH32 AH34 AH36 AH38 AH40 AH42 AH44 AH49 AH51 AH53 AH55 AH57 AJ13 AJ14 AJ23 AJ25 AJ27 AJ29 — VSS

AJ35 AJ39 AJ41 AJ43 AJ45 AJ47 AJ50 AJ52 AJ54 AJ56 AJ58 AJ60 AJ63 AK23 AK3 AK52 AL10 AL13 AL17 AL20 AL22 AL23 AL26 AL29 AL31 AL33 AL36 AL39 AL40 AL45 AL46 AL51 AL52 AL54 AL57 AL60 AL61 AM1 AM17 AM23 AM31 AM52 AN17 AN23 AN31 AN32 AN35 AN36 AN39 AN40 AN42 AN43 AN45 AN46 AN48 AN49 AN51 AN52 AN60 AN63 AN7 AP10 AP17 AP20

14 OF 19

@UCPU1O BDW_ULT_DDR3L

AP22 AP23 AP28 AP29 AP3 AP31 AP38 AP39 AP48 AP52 AP54 AP57 AR11 AR15 AR17 AR23 AR31 AR33 AR39 AR43 AR49 AR5 AR52 AT13 AT35 AT37 AT40 AT42 AT43 AT46 AT49 AT61 AT62 AT63 AU1 AU16 AU18 AU20 AU22 AU24 AU26 AU28 AU30 AU33 AU51 AU53 AU55 AU57 AU59 AV14 AV16 AV20 AV24 AV28 AV33 AV34 AV36 AV39 AV41 AV43 AV46 AV49 AV51 AV55 — VSS

AV59 AV8 AW16 AW24 AW33 AW35 AW37 AW4 AW40 AW42 AW44 AW47 AW50 AW51 AW59 AW60 AY11 AY16 AY18 AY22 AY24 AY26 AY30 AY33 AY4 AY51 AY53 AY57 AY59 AY6 B20 B24 B26 B28 B32 B36 B4 B40 B44 B48 B52 B56 B60 C11 C14 C18 C20 C25 C27 C38 C39 C57 D12 D14 D18 D2 D21 D23 D25 D26 D27 D29 D30 D31

15 OF 19

@UCPU1P BDW_ULT_DDR3L

D33 D34 D35 D37 D38 D39 D41 D42 D43 D45 D46 D47 D49 D5 D50 D51 D53 D54 D55 D57 D59 D62 D8 E11 E17 F20 F26 F30 F34 F38 F42 F46 F50 F54 F58 F61 G18 G22 G3 G5 G6 G8 H13 — VSS

H17 H57 J10 J22 J59 J63 K1 K12 L13 L15 L17 L18 L20 L58 L61 L7 M22 N10 N3 P59 P63 R10 R22 R8 T1 T58 U20 U22 U61 U9 V10 V3 V7 W20 W22 Y10 Y59 Y63 V58 AH46 V23 E62 AH16 — VSS

VSS_SENSE

16 OF 19

RC99 & RC100 close to PCH

RC100 1 2 100_0402_1%~D VSSSENSE [47]

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

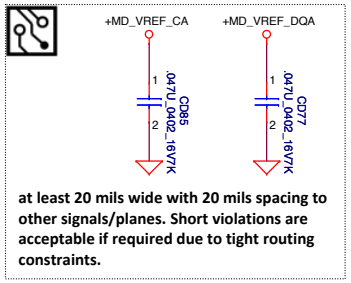
Compal Electronics, Inc.

Title: P14-MCP(10/10) PWR,VSS,CFG

Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 Sheet 14 of 50

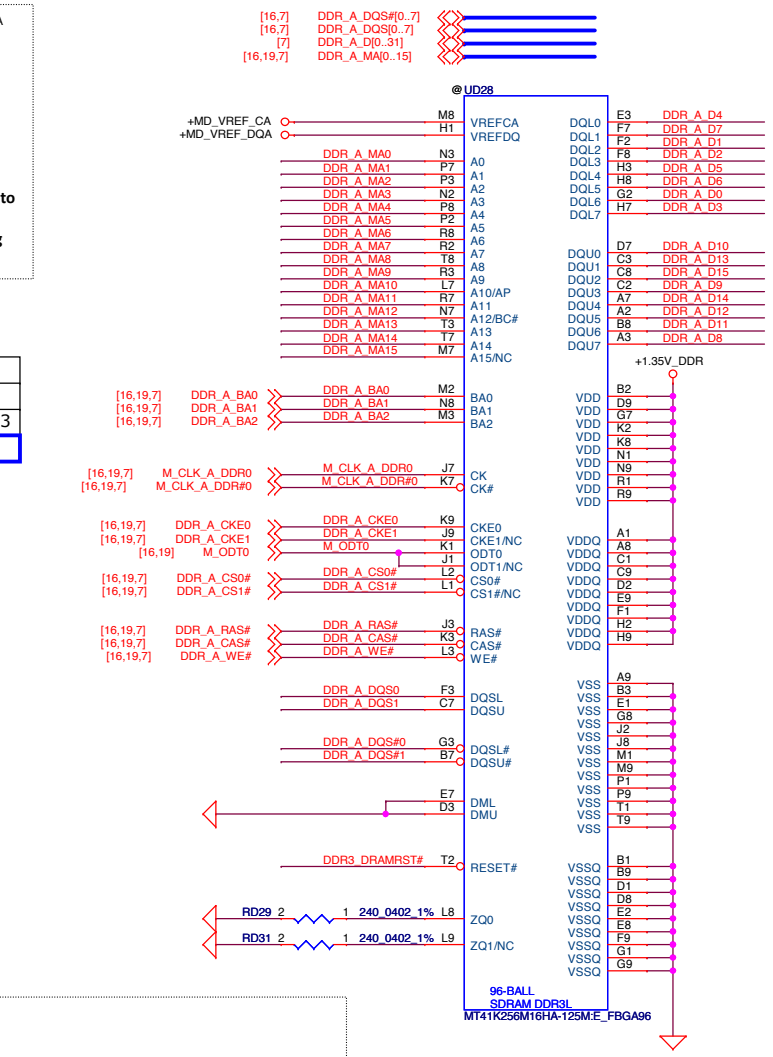
CHA DDR3L Memory Down Lower Bits

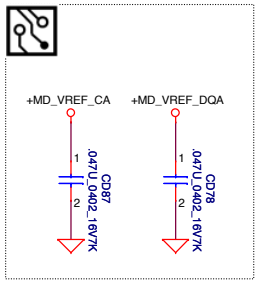


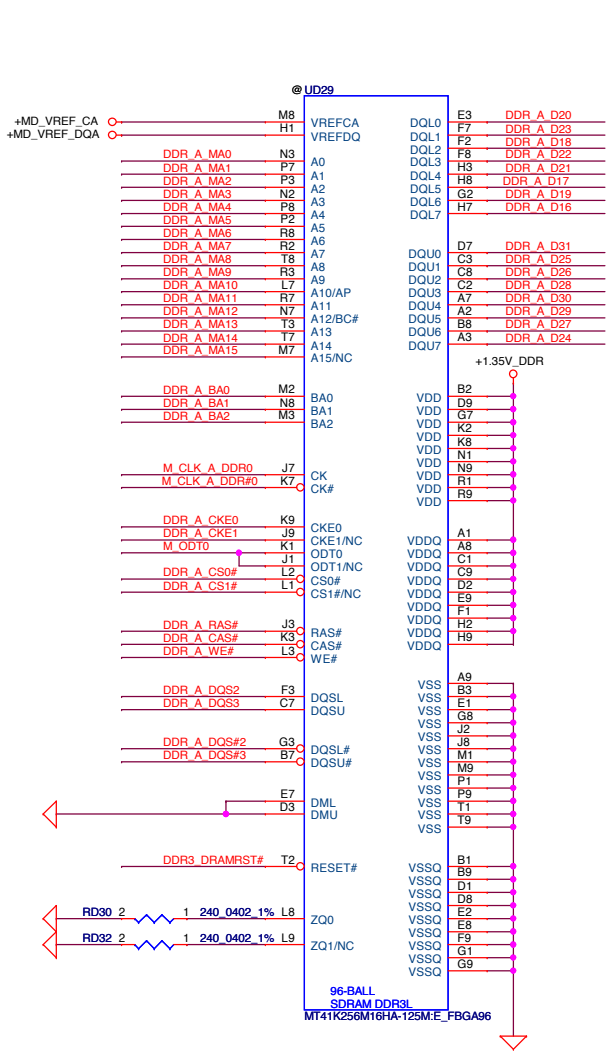
at least 20 mils wide with 20 mils spacing to other signals/planes. Short violations are acceptable if required due to tight routing constraints.

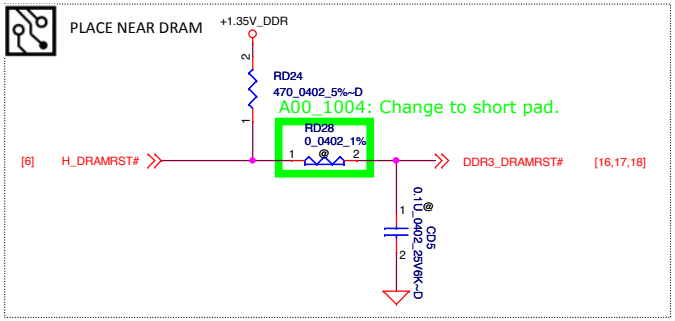
DDR3L Package (mm^2)

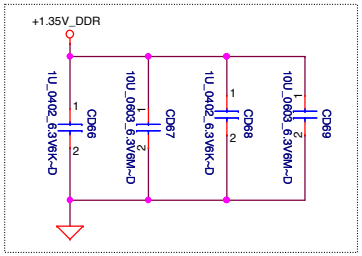
	4G	8G
Hynix	9 x 13	TBD
Samsung	10 x 13	11 x 13.3
Micron	9 x 14	10 x 14

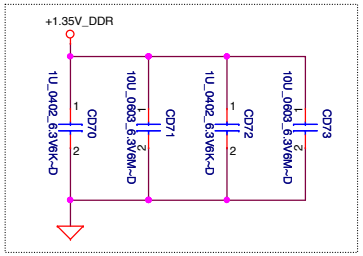












Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28

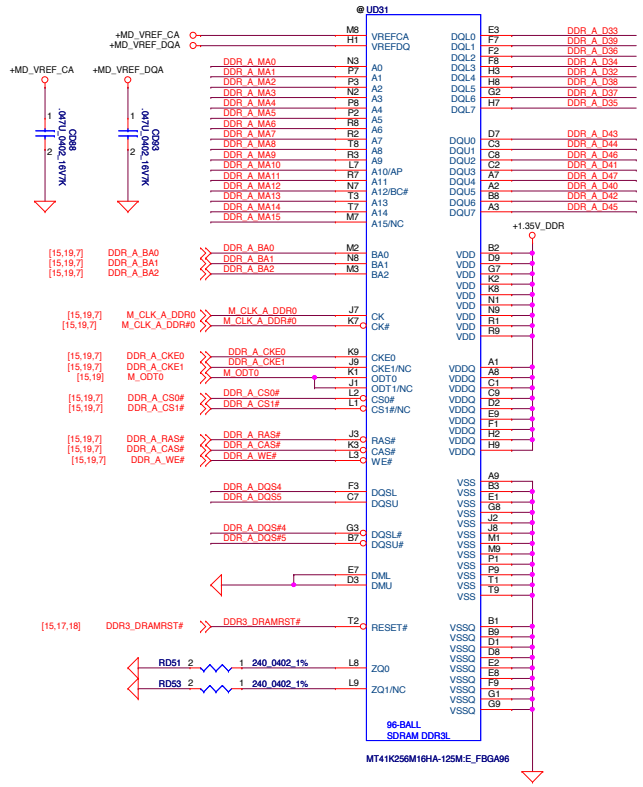
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

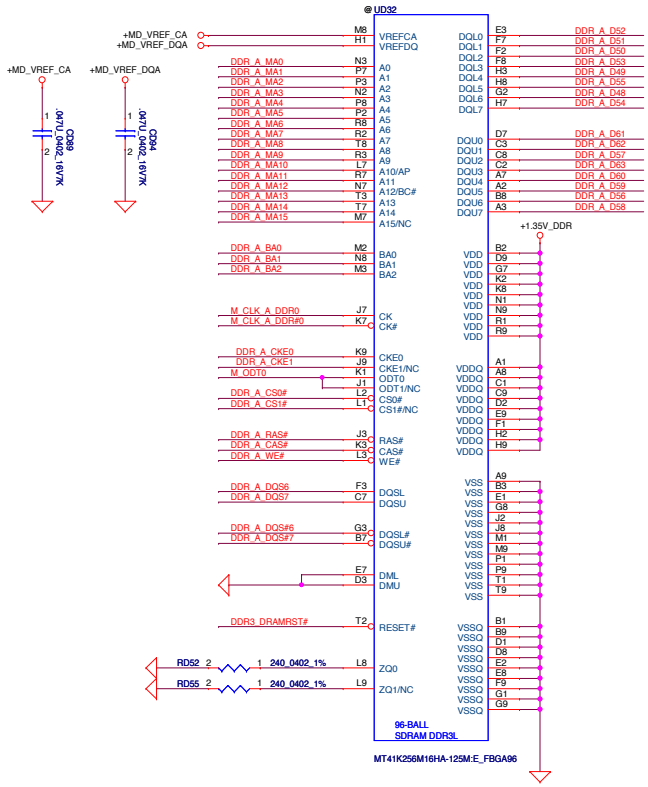
Title	P12-DDRIII Channel A		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Sunday, October 05, 2014	Sheet	15 of 50

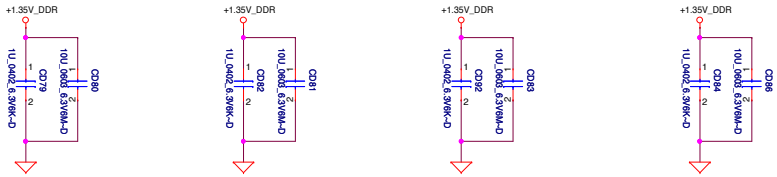
CHA DDR3L Memory Down Upper Bits

[15,7] DDR_A_DQS#[0..7]
[15,7] DDR_A_DQS[0..7]
[7] DDR_A_D[32..63]
[15,19,7] DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width







Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

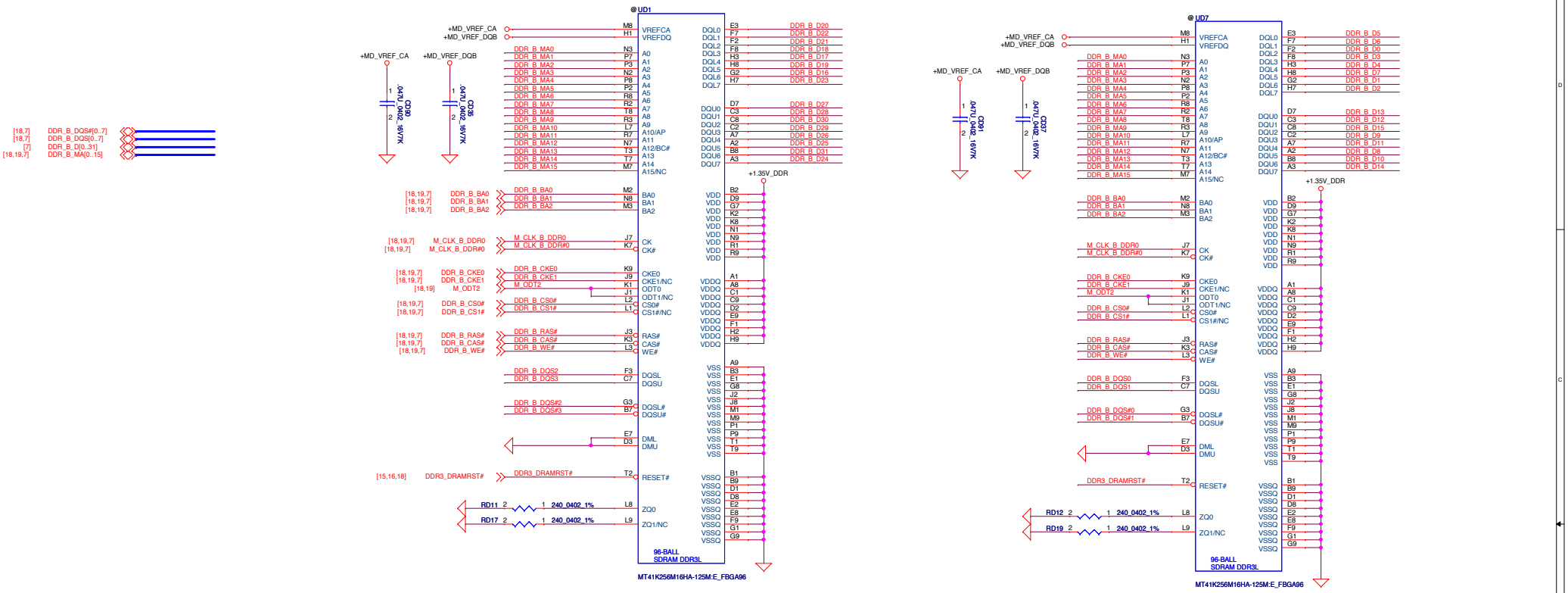
Compal Electronics, Inc.

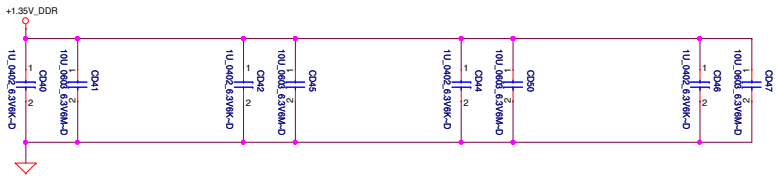
Title: P13-DDRIII Channel A

Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 Sheet 16 of 50

CHB DDR3L Memory Down Lower Bits





Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

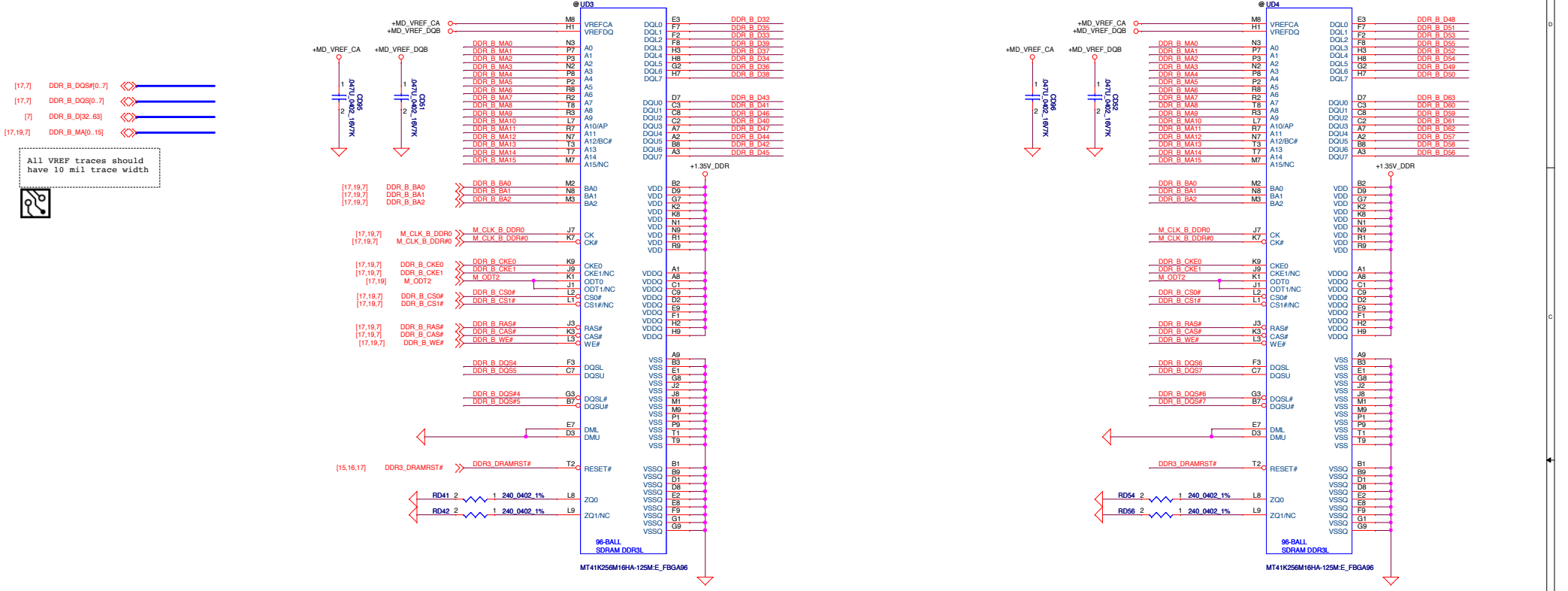
Compal Electronics, Inc.

Title: P14-DDRIII Channel B

Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 | Sheet 17 of 50

CHB DDR3L Memory Down Upper Bits



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

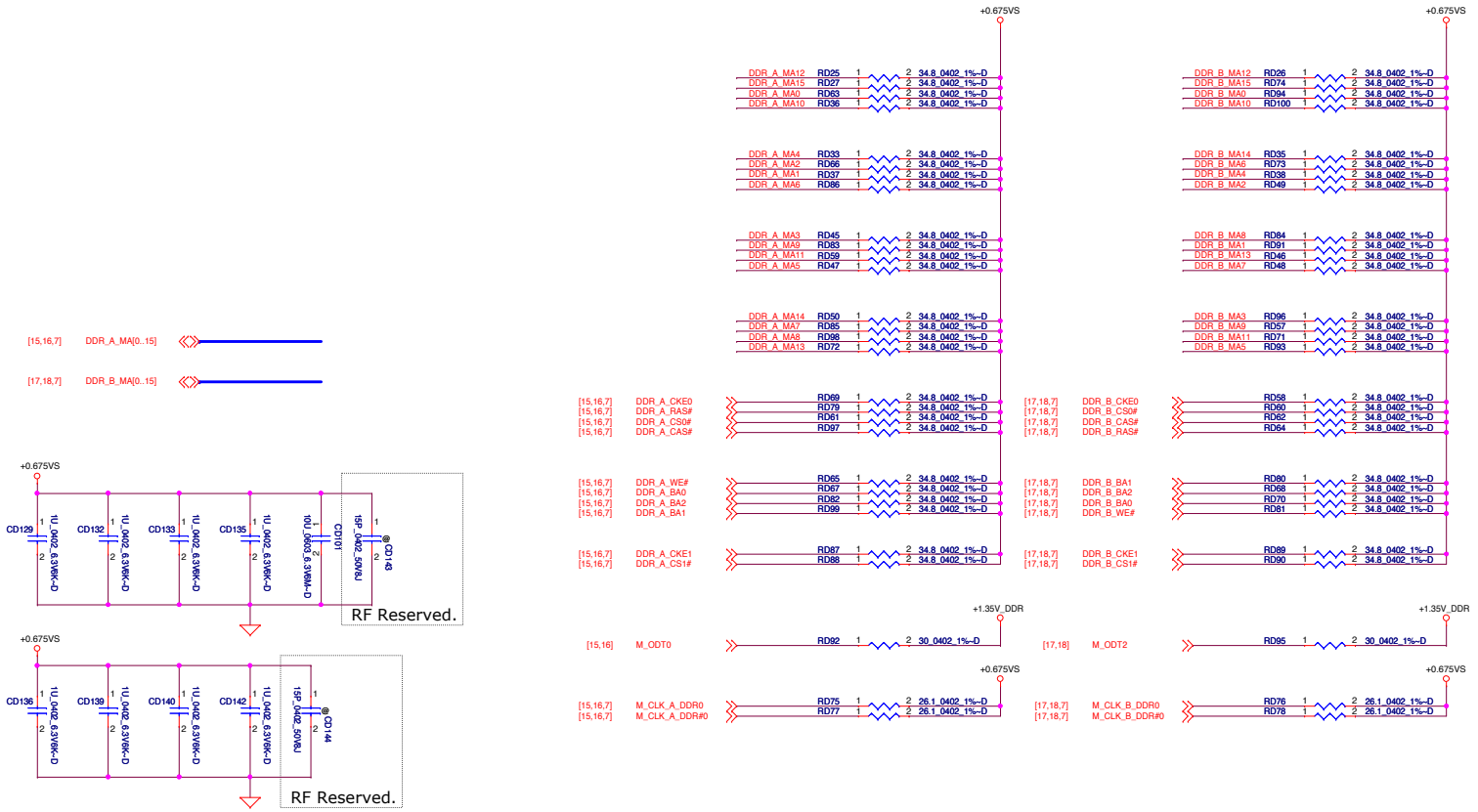
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

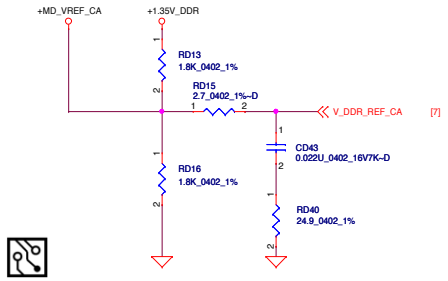
Title: P15-DDRIII Channel B

Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 Sheet 18 of 50

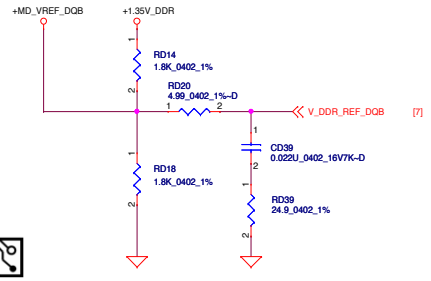


Channel A/B CA VREF



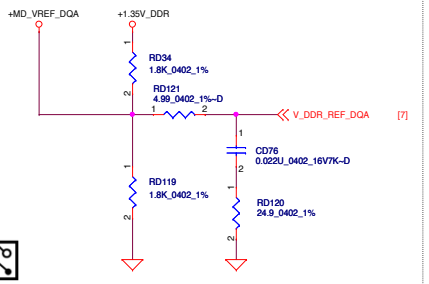
Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

Channel B DQ VREF



Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

Channel A DQ VREF



Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

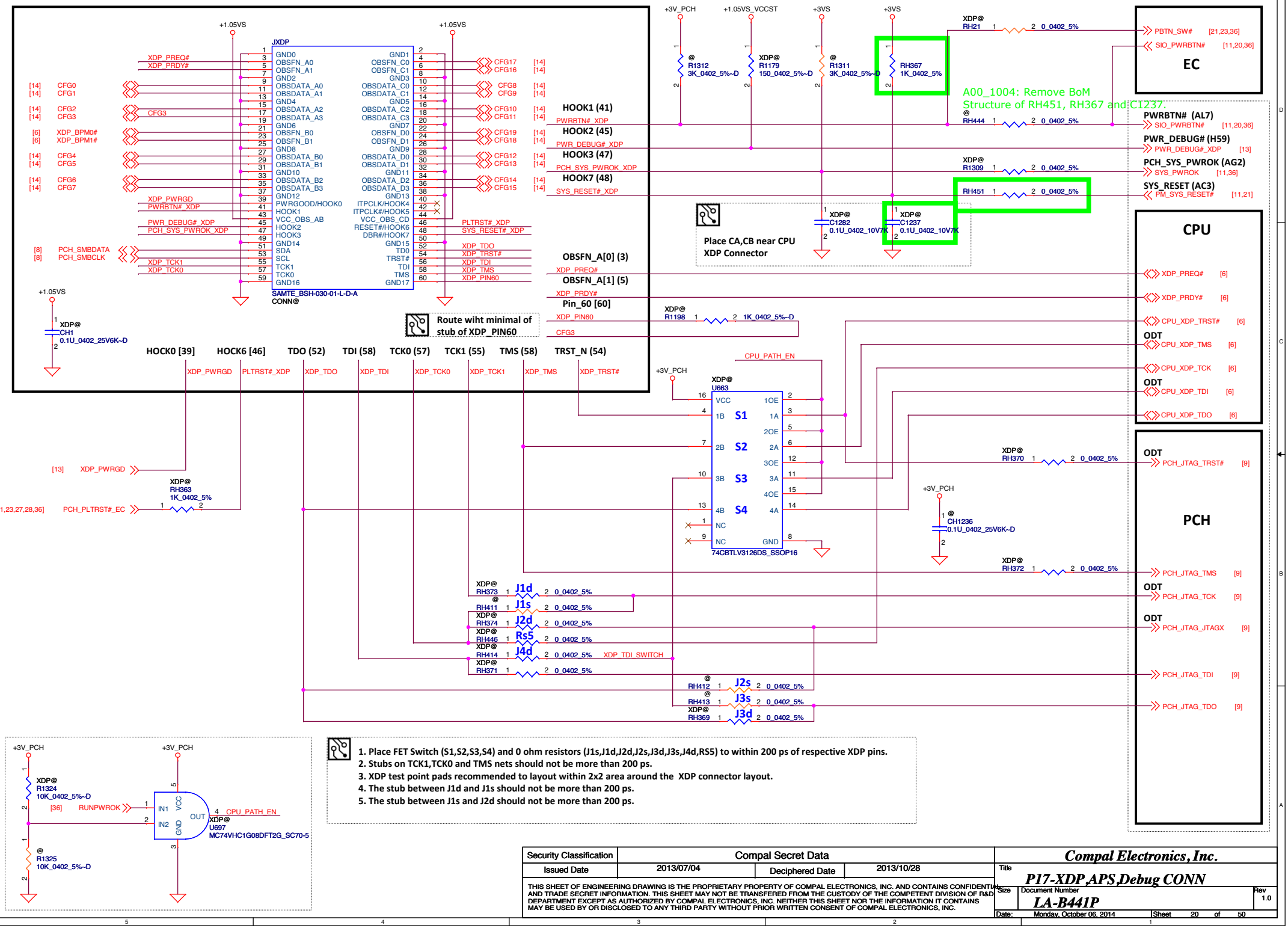
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P16-DDRIII Channel B

Size | Document Number: LA-B441P | Rev: 1.0

Date: Saturday, October 04, 2014 | Sheet 19 of 50

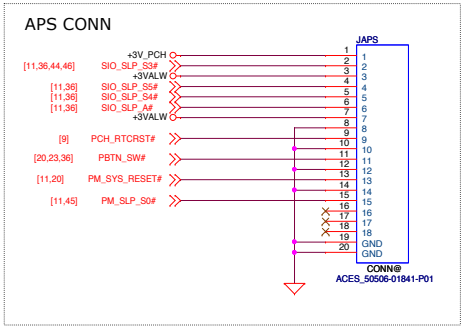


Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

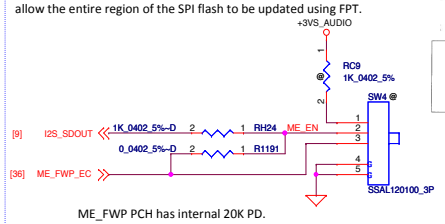
Compal Electronics, Inc.			
Title: P17-XDP,APS,Debug CONN			
Size	Document Number: LA-B441P		Rev: 1.0
Date: Monday, October 06, 2014		Sheet 20 of 50	

APS CONN



A00_1004: Depop SW4, RC9; pop R1191.

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

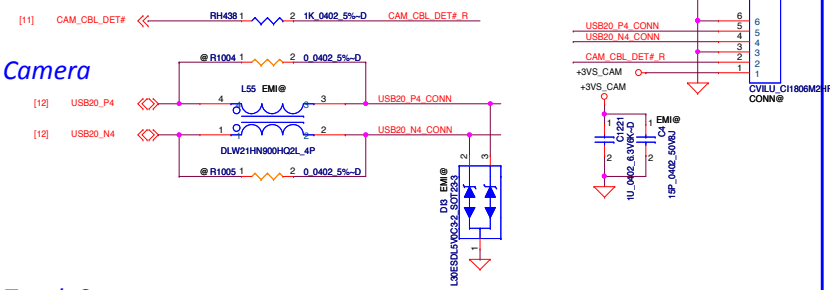
Compal Electronics, Inc.

Title: **P18-BLANK**

Size | Document Number: **LA-B441P** | Rev: 1.0

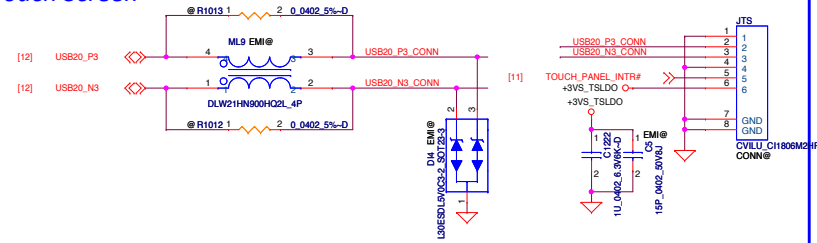
Date: Monday, October 06, 2014 | Sheet 21 of 50

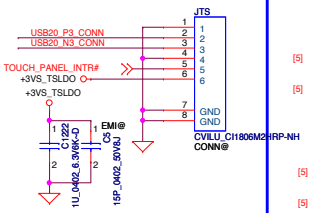
Camera + Touch Screen



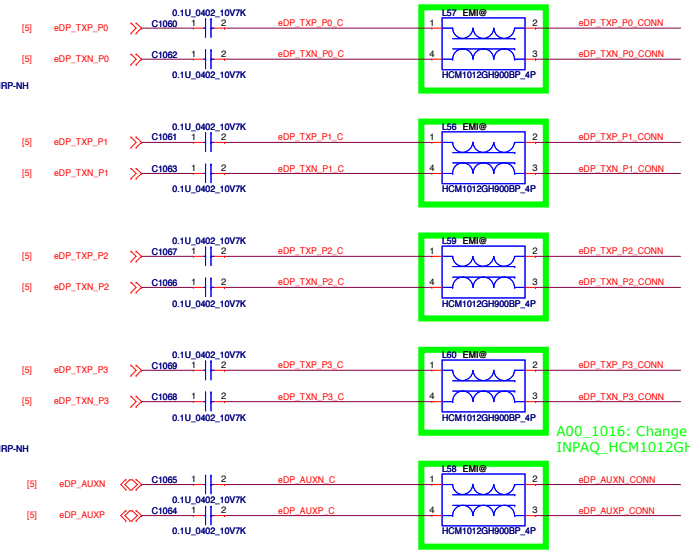
Camera

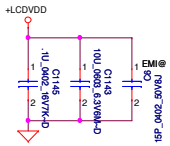
Touch Screen

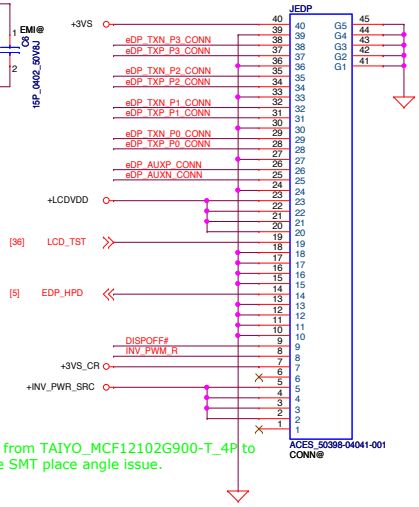




eDP Conn

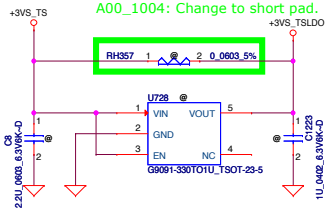




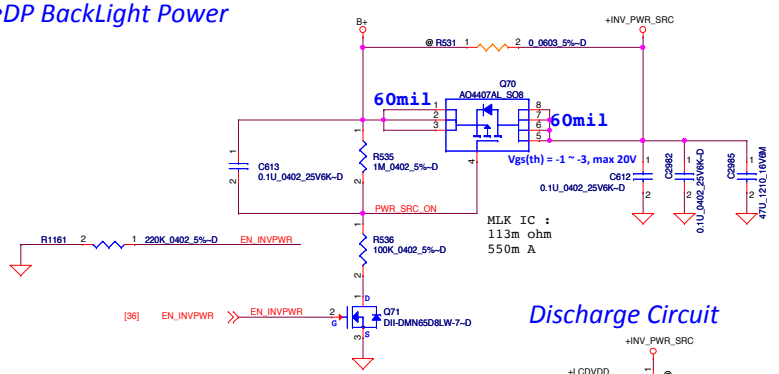


A00_1016: Change L56~L60 footprint from TAIYO_MCF12102G900-T_4P to INPAQ_HCM1012GH900BP_4P to solve SMT place angle issue.

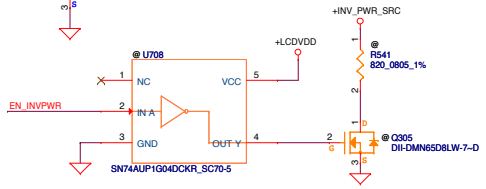
Touch Screen LDO



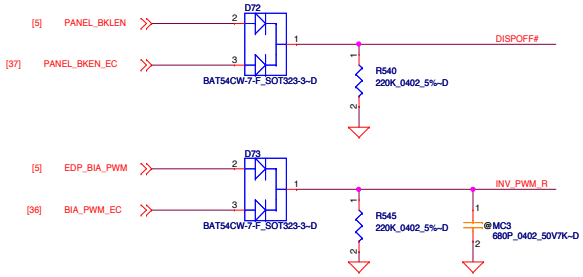
eDP BackLight Power



Discharge Circuit



BackLight PWM Control



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

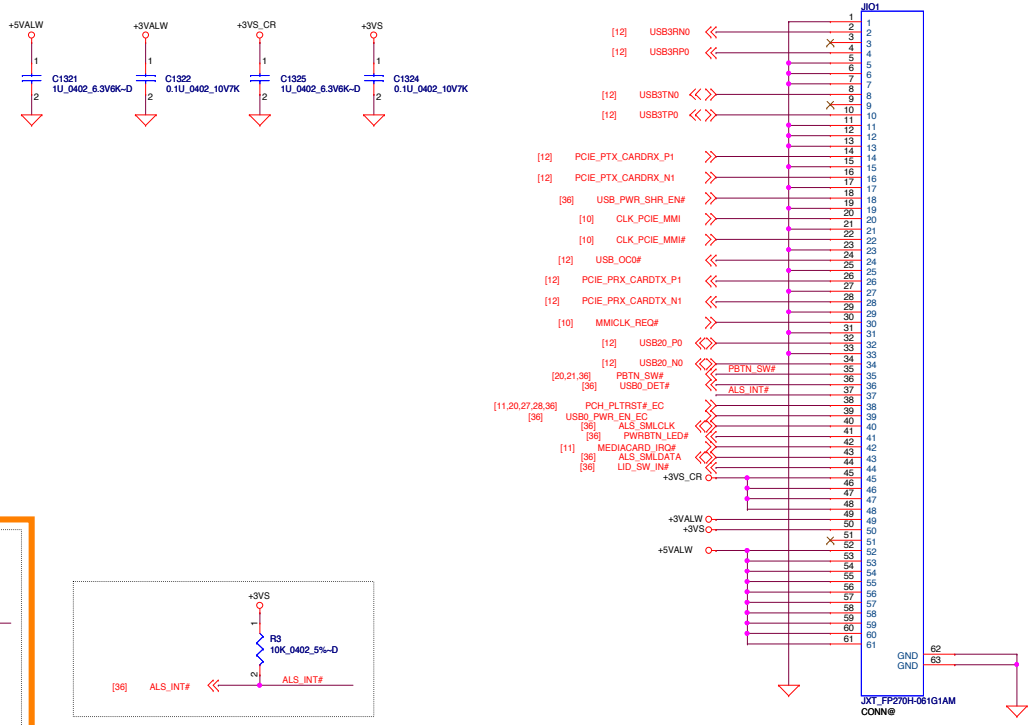
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

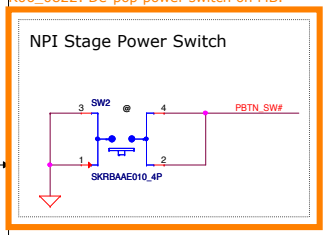
Title: P19-eDP/ Camera CONN

Size | Document Number: LA-B441P | Rev: 1.0

Date: Thursday, October 16, 2014 | Sheet 22 of 50



R06_0822: De-pop power switch on MB.



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **P20-BTB CONN & Battery LED**

Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 | Sheet 23 of 50

HD Audio Codec

A00_1004: Change to short pad.

RA45 close with UA2.53

Codec
Analog
Pin20~45
Digital
Pin1~19, 46~56

UA2
ALC3263-CG_QFN56_7X7

Beep sound

Close to UA2 Pin2

For EMI

CA42,CA31 close with UA2.7

CA105,CA104 close with UA2.19

HDA_I2S_SEL = Low ; HDA Mode
HDA_I2S_SEL = High ; I2S Mode

HD_SOC_SEL = Low ; I2S Mode
HD_SOC_SEL = High ; HDA Mode

RA11,CA26 Close UA2 Pin6

CA18 close UA2 Pin12

Close to UA2

Reserved for EMI

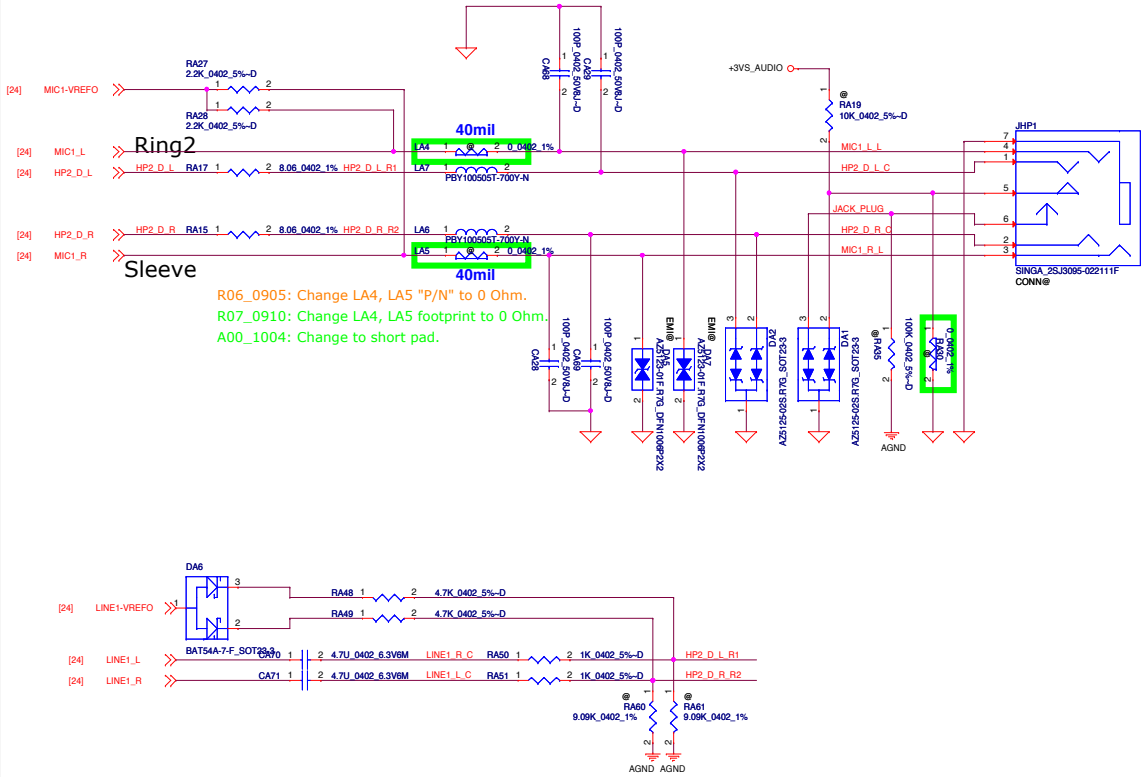
Reserved for EMI

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28

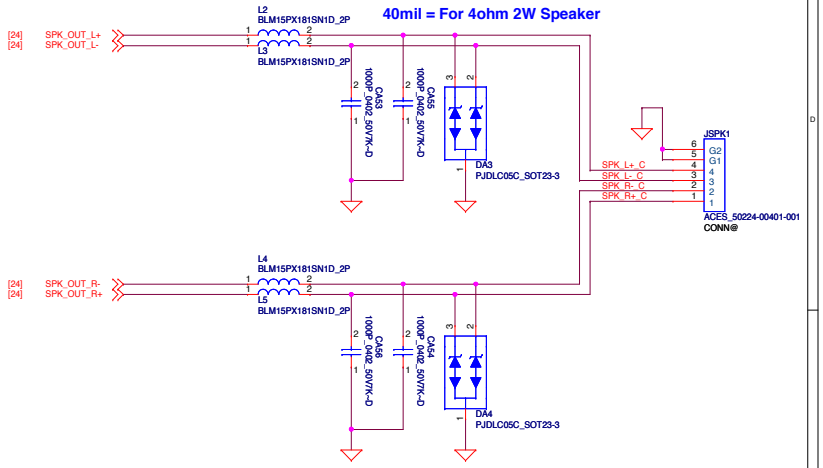
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title: P21-Audio Codec
Size: | Document Number: LA-B441P | Rev: 1.0
Date: Sunday, October 05, 2014 | Sheet 24 of 50

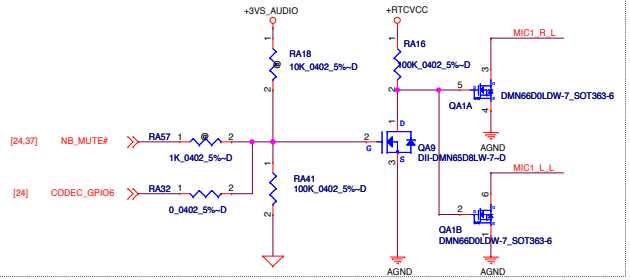
Universal Audio Jack



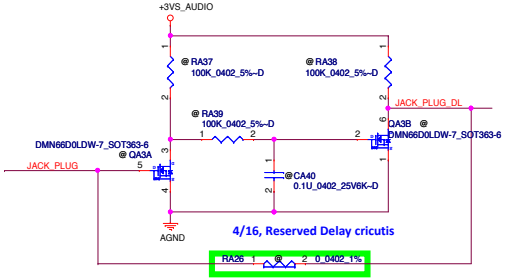
Int. Speaker Conn.



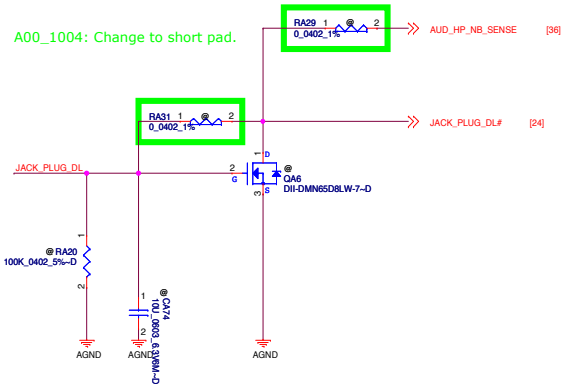
Prevent S3/S4/S5 Background Noise.



Reserved Delay cricutis



A00_1004: Change to short pad.



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

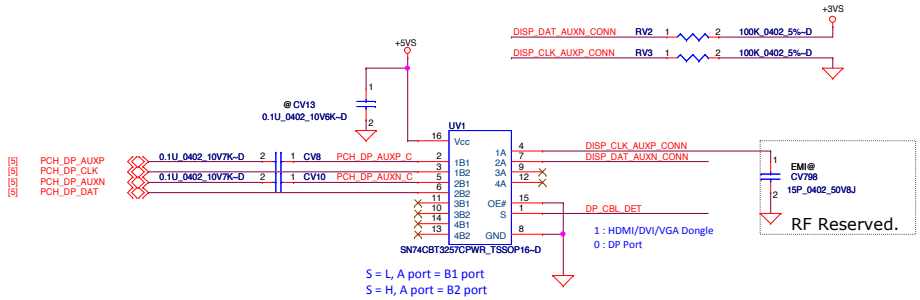
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

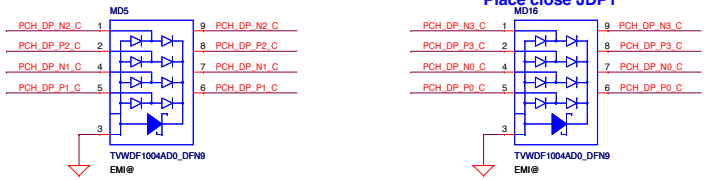
Title: **P22-Audio Conn**

Size	Document Number	Rev
	LA-B441P	1.0

Date: Monday, October 06, 2014 | Sheet 25 of 50

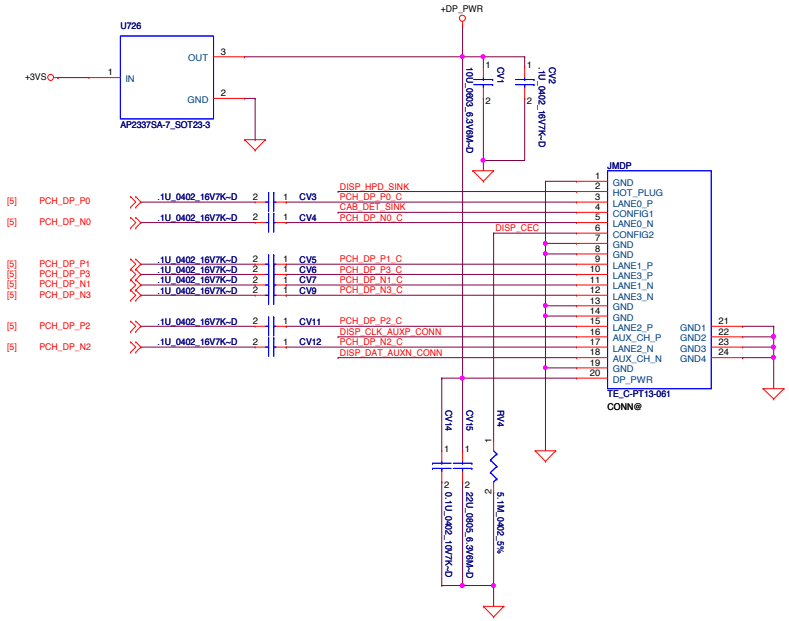


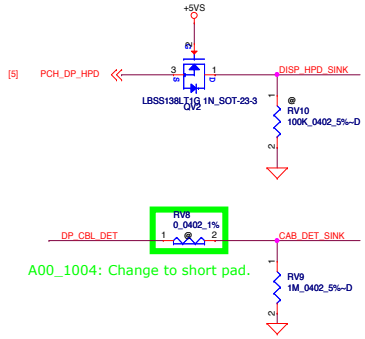
DP Signal ESD



Place close JDP1

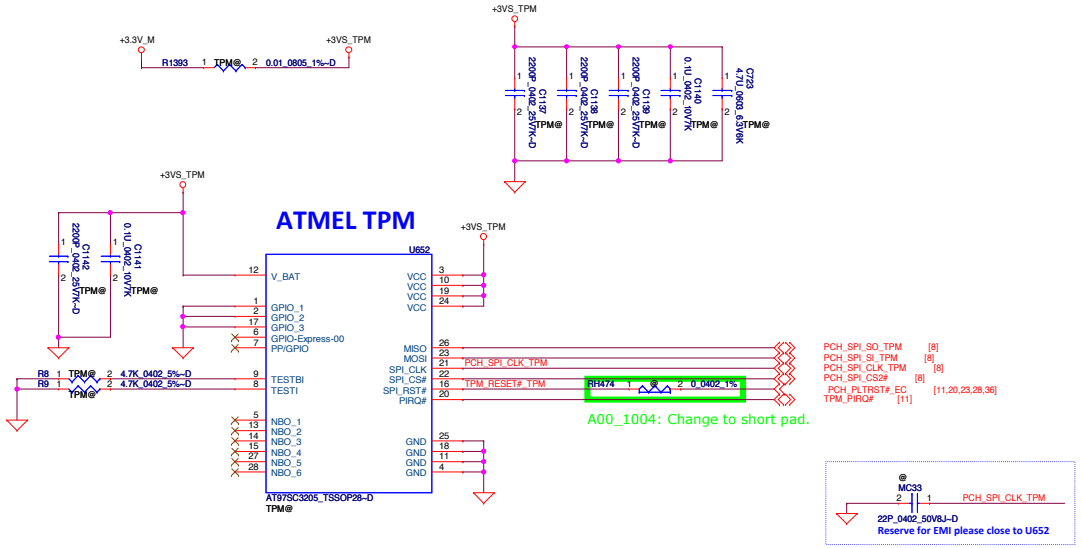
Mini DP CONN





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28
Title	P23-Mini DP CONN		
Size C	Document Number LA-B441P		Rev 1.0
Date: Sunday, October 05, 2014	Sheet 26 of 50		

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

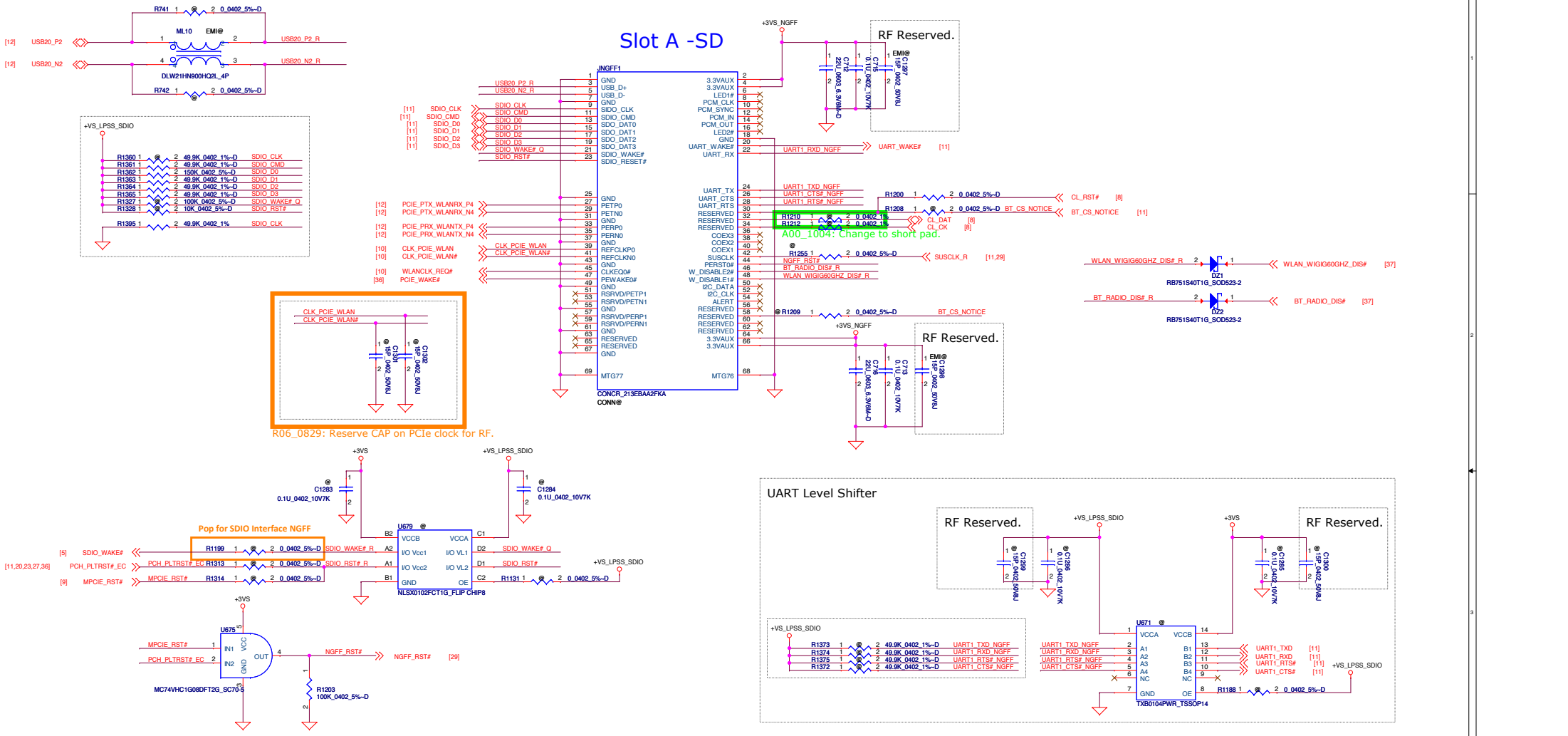


Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title: P24-TPM			
Size	Document Number: LA-B441P		Rev: 1.0
Date: Sunday, October 05, 2014	Sheet 27 of 50		

Wireless LAN

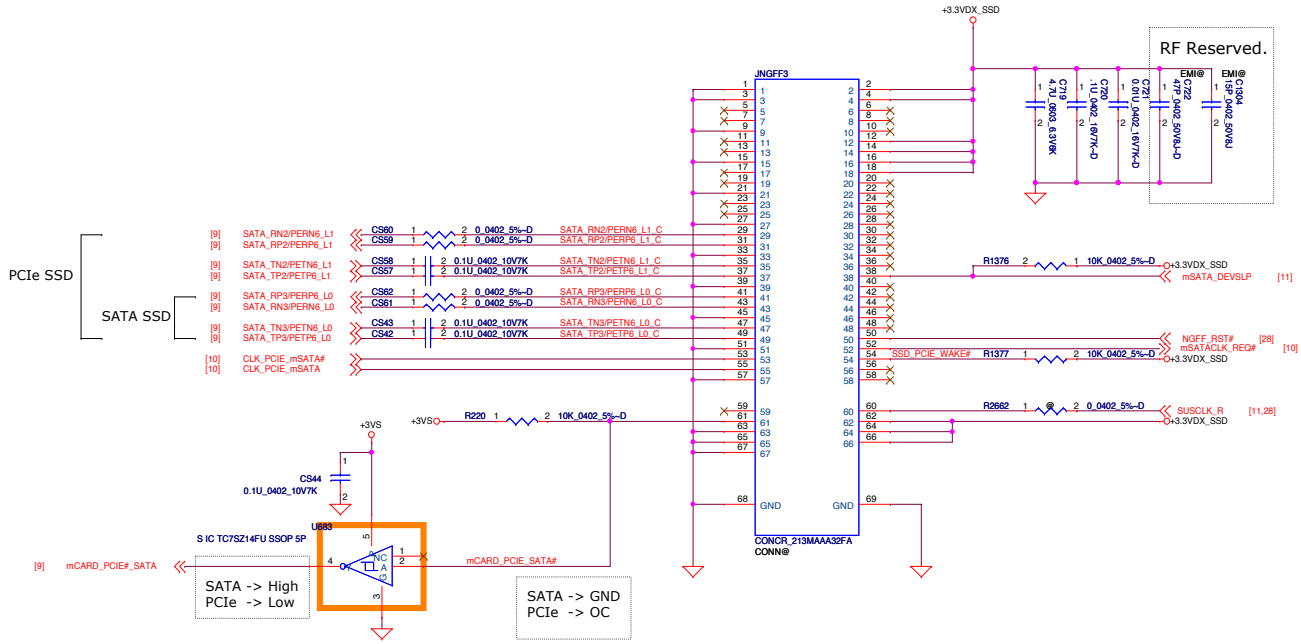


Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

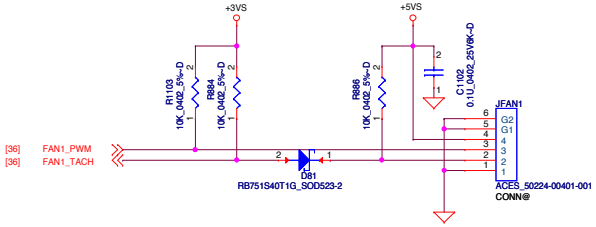
Compal Electronics, Inc.			
Title	P25-WLAN / BT (M.2)		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Sunday, October 05, 2014	Sheet	28 of 50

M.2 Slot-C Key-M (SSD)

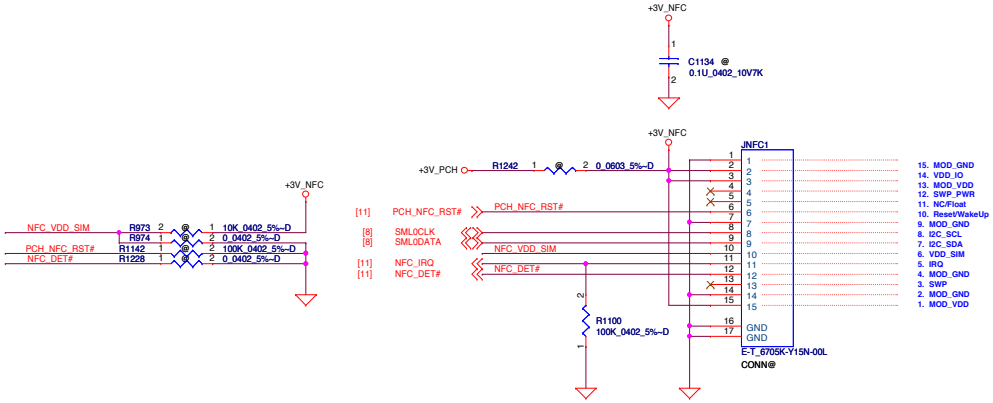


R06_0902: Main source has been banned by sourcer. change main source from SA00001N400 to SA00001N200.

FAN



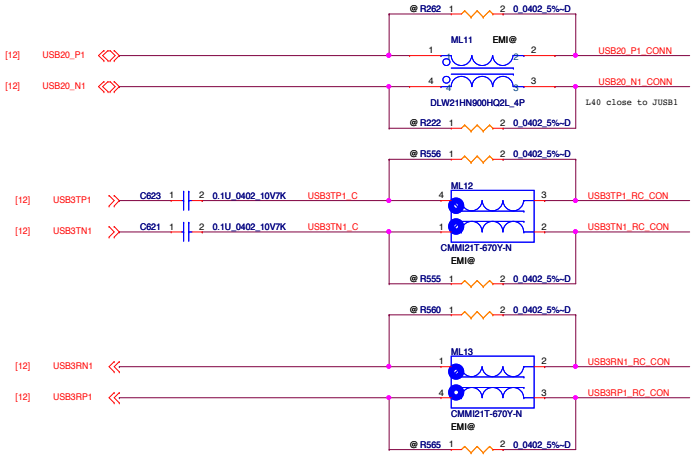
NFC(Reserved)

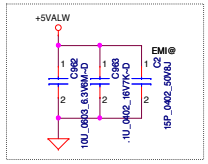


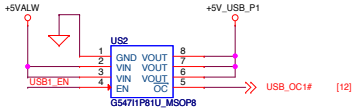
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date 2013/10/28	Title: P26-mSATA / NFC / FAN Conn
Size: C	Document Number: LA-B441P		Rev: 1.0
Date: Saturday, October 04, 2014	Sheet 29 of 50		

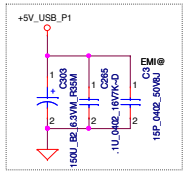
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

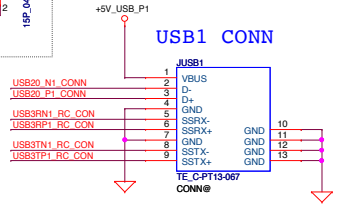
USB IO Port



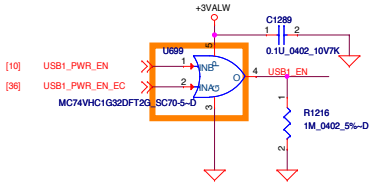


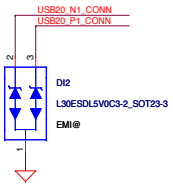


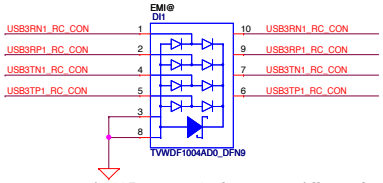




R06_0822: Change P/N to suffix '0'.

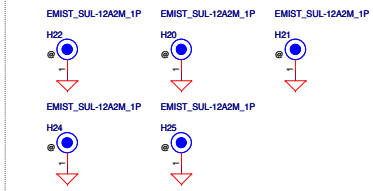






Hank0225: Note, PCB footprint is different from TVWDF1004AD0_DFN9, but it's compatible.

USB3.0 Shielding Clip



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

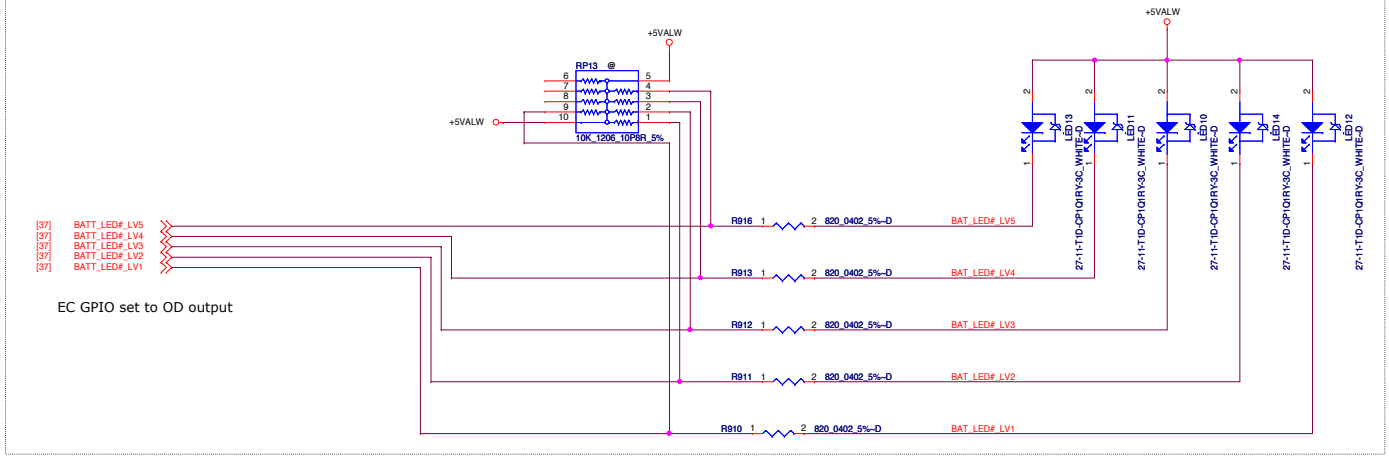
Compal Electronics, Inc.

Title: P27-USB 3.0 IO CONN

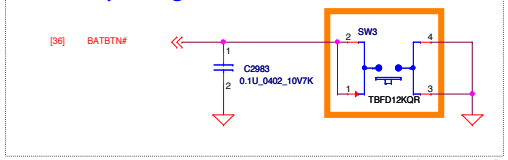
Size	Document Number	Rev
	LA-B441P	1.0

Date: Saturday, October 04, 2014 Sheet 30 of 50

Battery Gauge LED



Battery Gauge Button



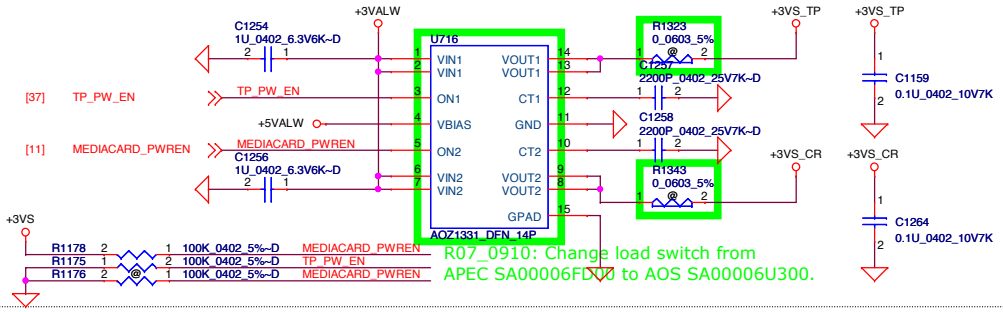
R06_0825: Change P/N form SN100006P00(MISAKI) to SN100008F00 as MISAKI has been banned.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28
Title	P28-BAT LED		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Saturday, October 04, 2014	Sheet	31 of 50

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Touch Pad, Card Reader Load Switch

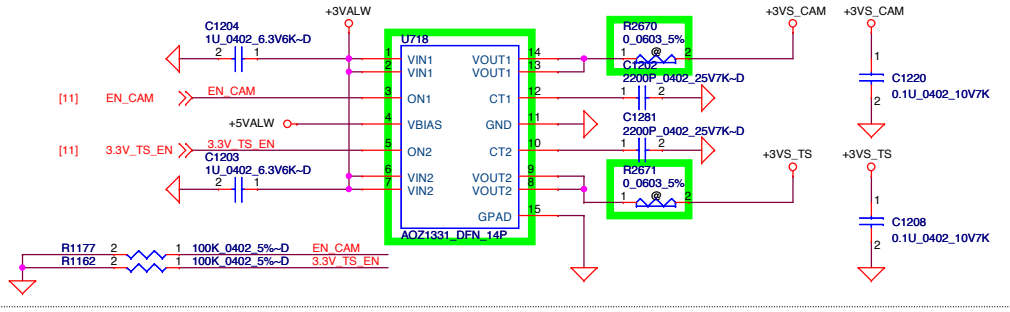
A00_1004: Change to short pad.



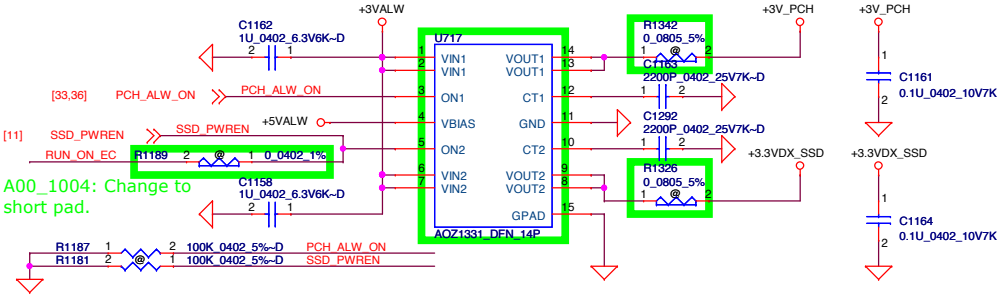
R07_0910: Change load switch from APEC SA00006FD00 to AOS SA00006U300.

Camera, Touch Screen Load Switch

A00_1004: Change to short pad.

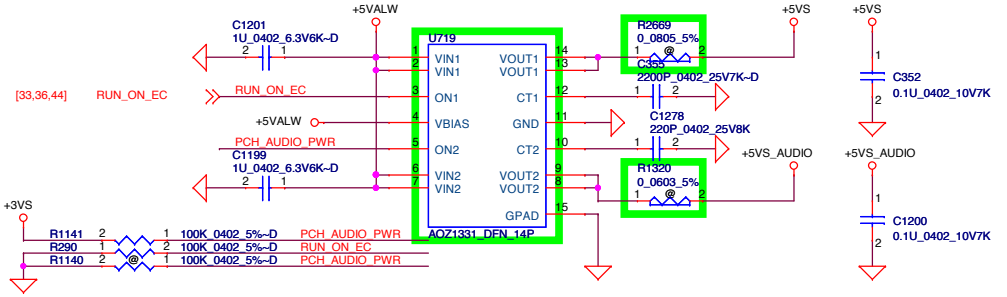


Deeper Sleep, SSD Load Switch

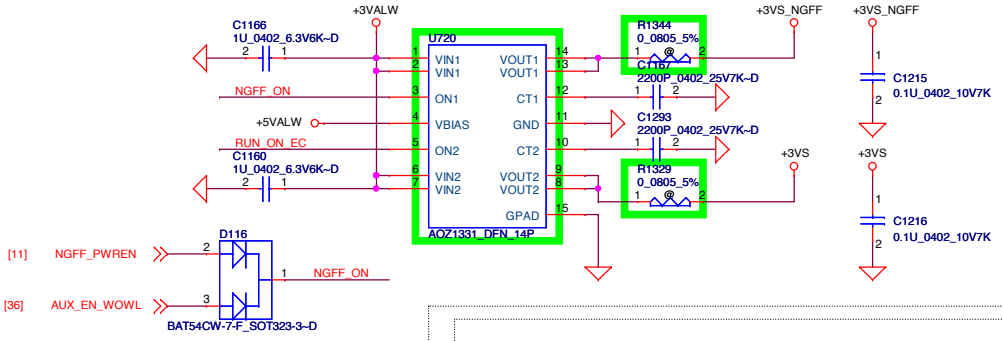


A00_1004: Change to short pad.

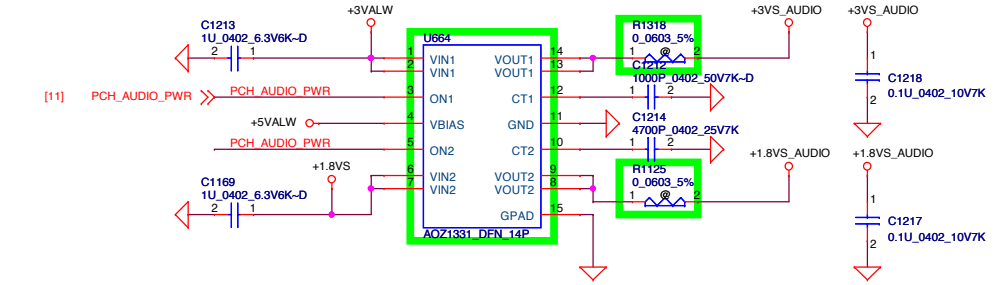
5V_Run, 5V_Audio Load Switch



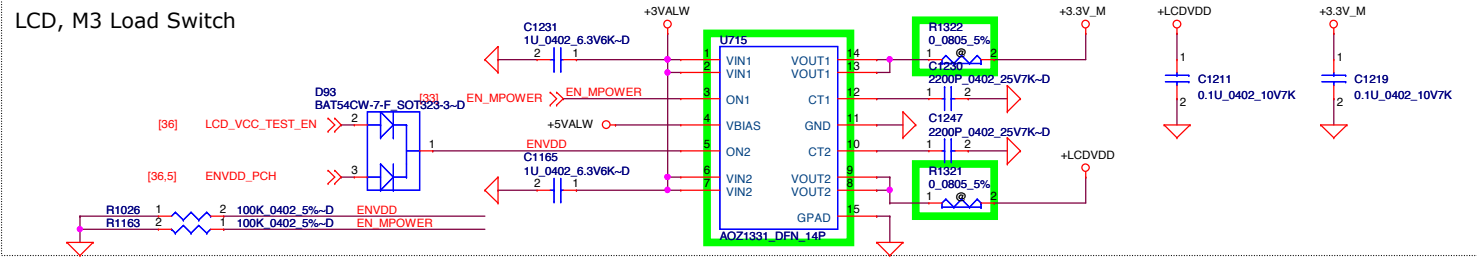
WiFi, 3V_RUN Load Switch



3V_Audio, 1.8V_Audio Load Switch



LCD, M3 Load Switch



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

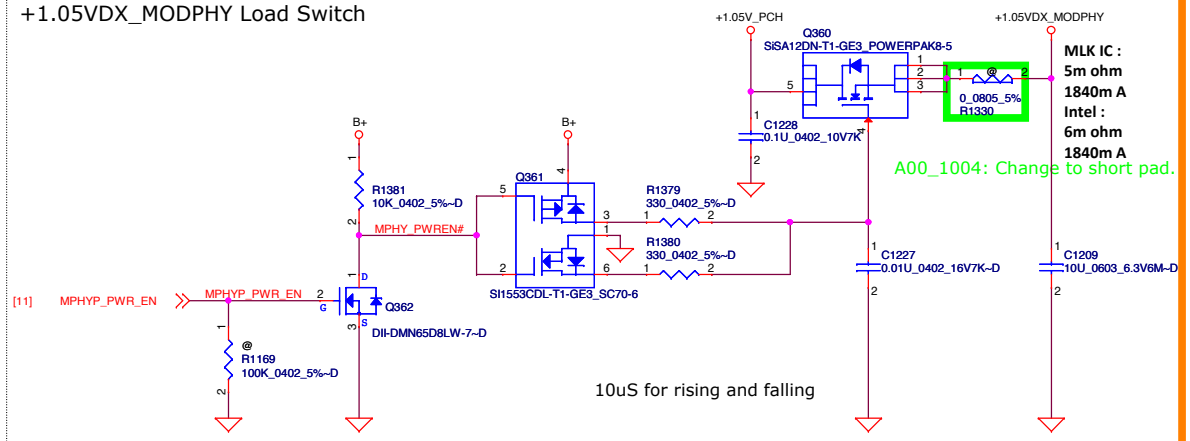
Compal Electronics, Inc.

Title: **P29-DC/DC Interface**

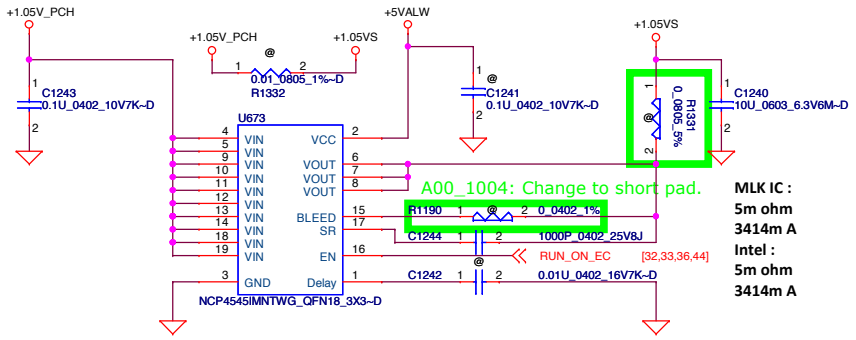
Size | Document Number: **LA-B441P** | Rev: 1.0

Date: Monday, October 06, 2014 | Sheet 32 of 50

+1.05VDX_MODPHY Load Switch

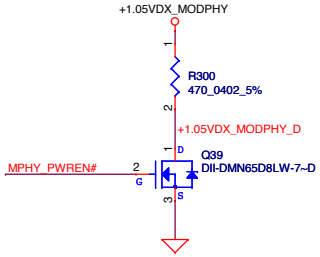


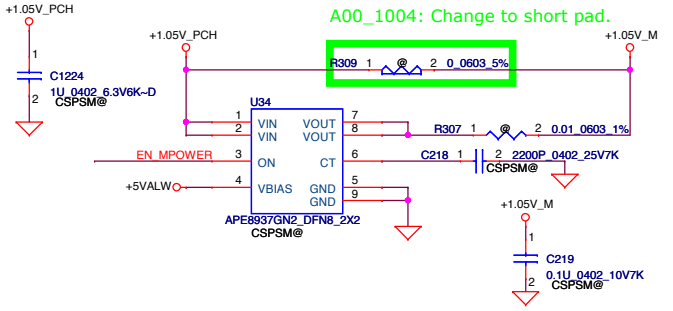
vPro Load Switch



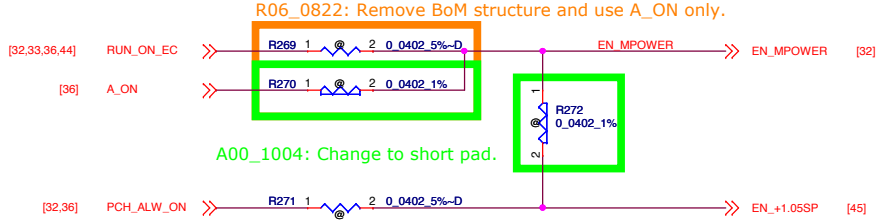
R06_1004: Remove BoM structure, both VPRO/Non-VPRO populated.

Discharge





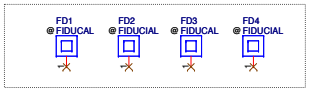
R06_0822: Remove BoM structure and use A_ON only.

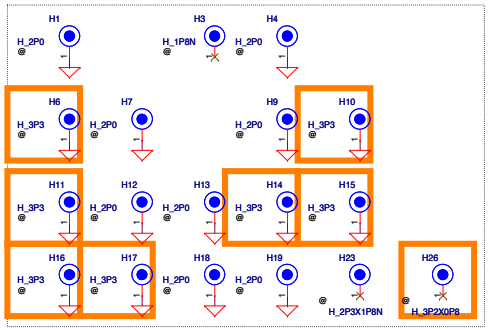


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

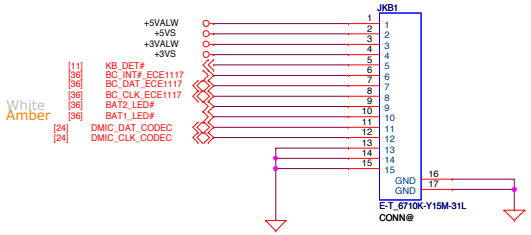
Title	P29-DC/DC Interface		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Monday, October 06, 2014	Sheet	33 of 50

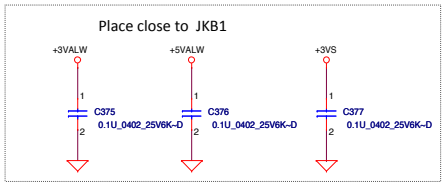




R06_0822: Stand off screw hole change form 3.2mm to 3.3 mm.
R06_0826: Add H26 for SSD bracket.

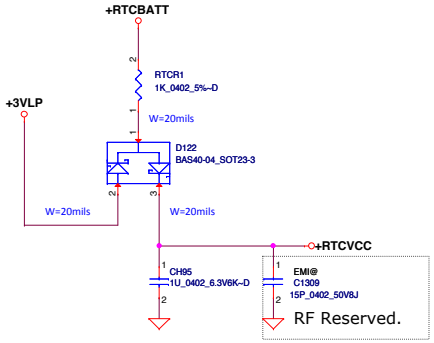
Keyboard Controller board + DMIC

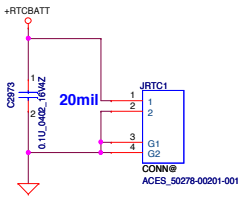


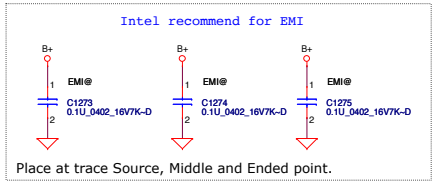


RTC Battery With Charge Function

RTC Battery Conn



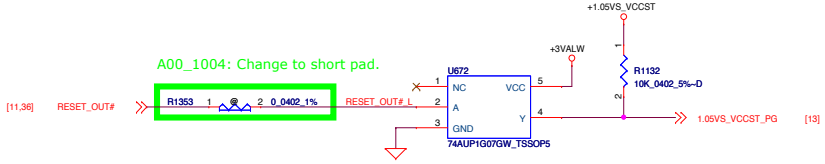




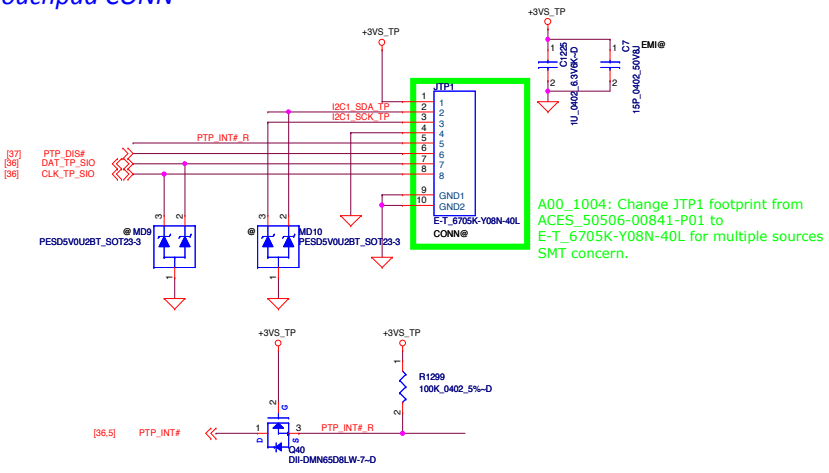
Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

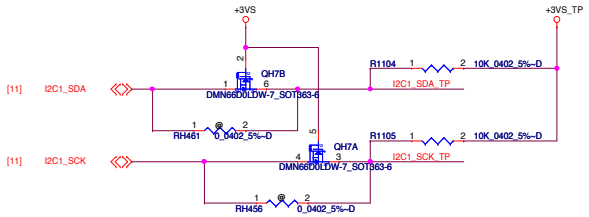
Compal Electronics, Inc.			
Title	P30-SCREWH/KB/RTC		
Size	Document Number		Rev
	LA-B441P		1.0
Date:	Saturday, October 04, 2014	Sheet	34 of 50



Touchpad CONN



A00_1004: Change JTP1 footprint from ACES_50506-00841-P01 to E-T_6705K-Y08N-40L for multiple sources SMT concern.



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **P31-TP/PWERGD/LID**

Size	Document Number	Rev
	LA-B441P	1.0

Date: Sunday, October 05, 2014 | Sheet 35 of 50

A00_1004: Change to short pad.

R06_0827: Change P/N to SA00006YH20.

Connect PCH, ALS

Connect Touch Pad

Connect Battery

Amber White

Charger

A00_1004: Change to short pad.

Connect ALS

R06_0826: Change RE55, RE56 form 10K to 8.2K as EA test result.

A00_1004: Change to short pad.

ESR <2ohms

R06_0905: Change YE1 main source form SJ100003R00 to SJ100003V00.
R06_1004: Change YE1 from SJ000003V00 to SJ100001A00.
Change CE62 form 27P to 22P and change CE53 form 33P to 27P.

32 KHz Clock

32.768KHZ 9PF Q13FC1350000300

Place close pin A29

EMI depop location

RE79	CE54	REV
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

A00_1004: Change board ID to A00.

Setting for Thermal Design

Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	BOT Skin2
DN2A/DP2A	BOT Skin1
DP3/DN3	DRAM
DP4/DN4	FAN

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

Rest=1.5K , Tp=88 degree

Place QE11 close to BOT Skin1 location
CE57 should close to QE11

Place QE4 close to BOT Skin2
CE48 should close to QE4

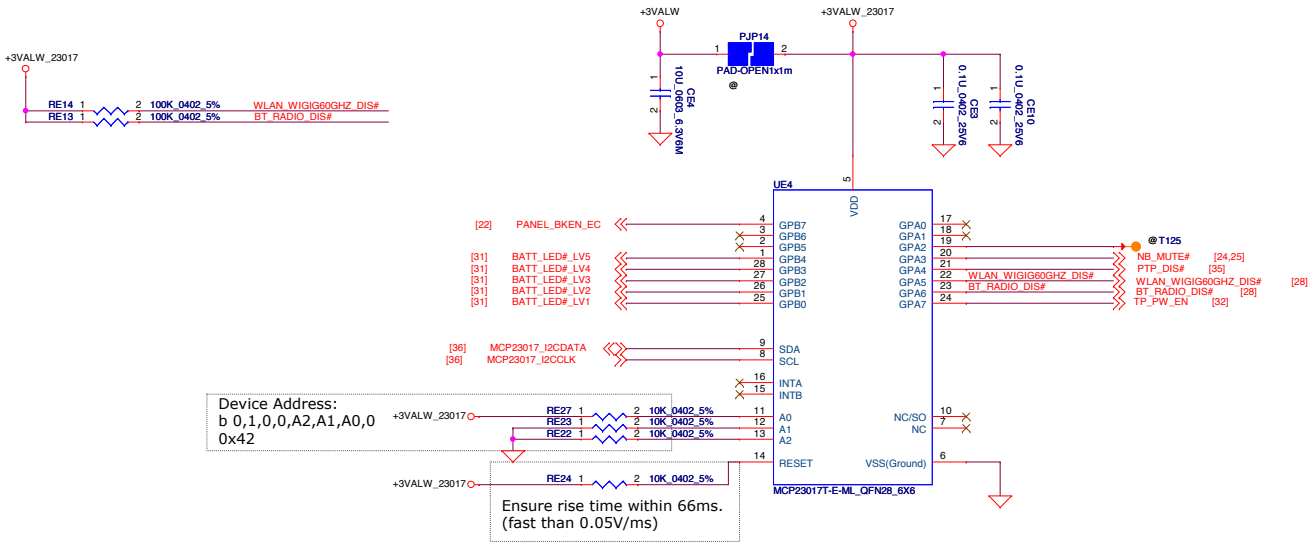
Place QE3 close to CPU
CE47 should close to QE3

Place QE10 close to DRAM
CE66 should close to QE10

Place QE8 close to FAN location
CE51 should close to QE8

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date 2013/10/28	Title: P32-EC ENE-KB9012
			Size: Document Number: LA-B441P Rev: 1.0
			Date: Sunday, October 05, 2014 Sheet 58 of 58

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

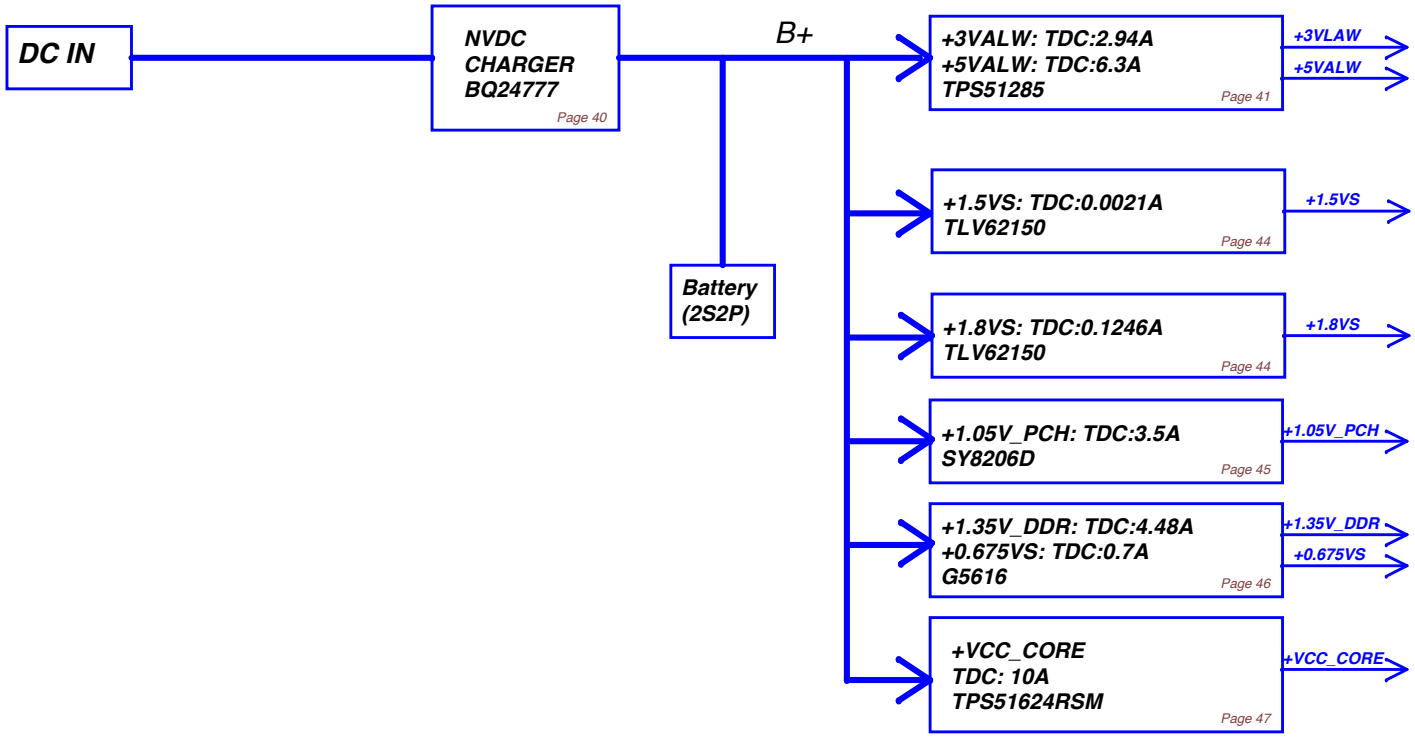
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P32-MCP23017

Size | Document Number: LA-B441P | Rev: 1.0

Date: Saturday, October 04, 2014 | Sheet 37 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

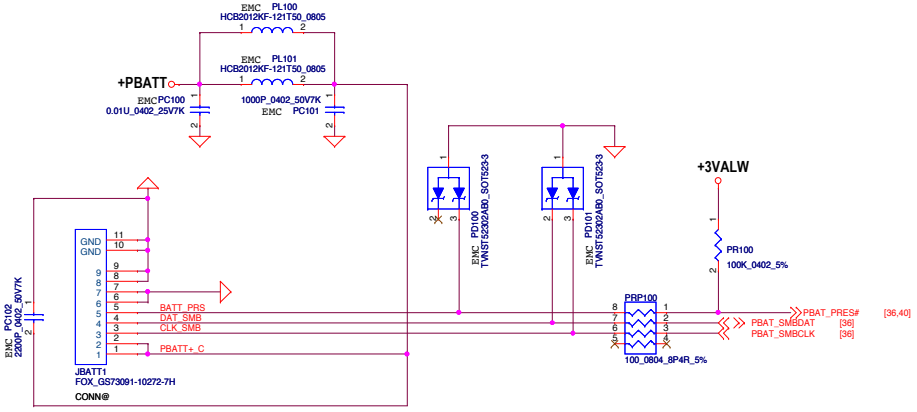
Compal Electronics, Inc.

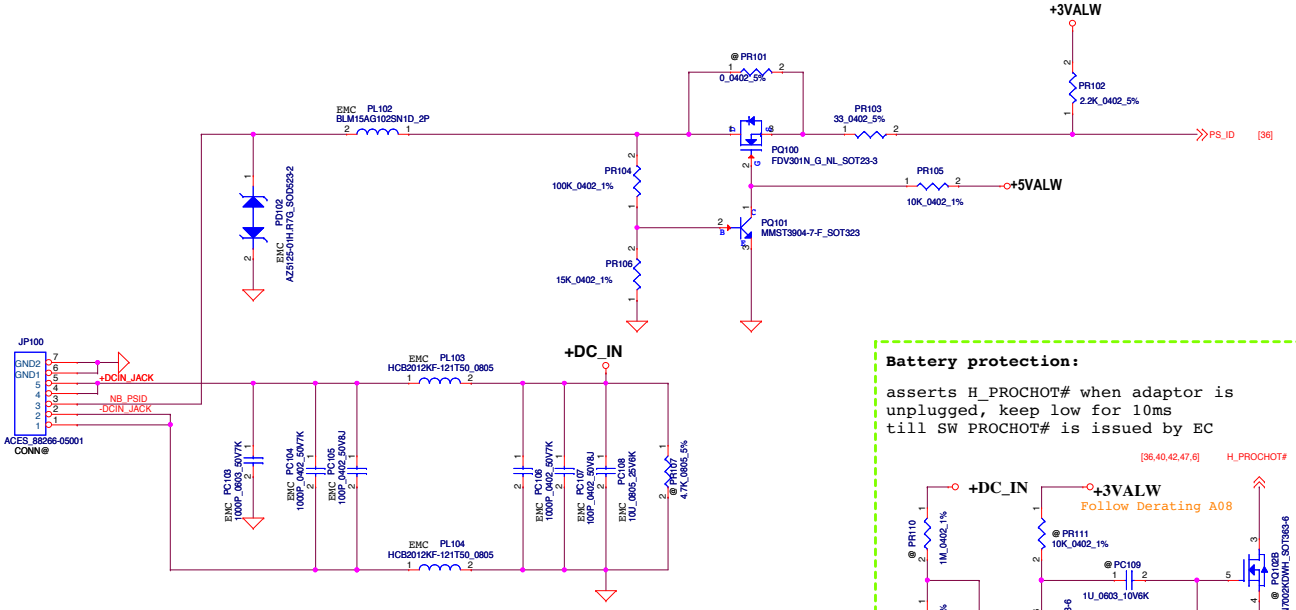
Title: P33-PWR_Block_Diagram

Size	Document Number	Rev
	LA-9261P	0.1

Date: Monday, October 06, 2014 Sheet 38 of 50

PBATT1 connector
SMART
Battery:
1.BATT++
2.BATT++
3.CLK_SMB
4.DAT_SMB
5.BAT_PRS
6.SYS_PRES
7.BAT_ALERT
8.GND
9.GND
10.GND
11.GND

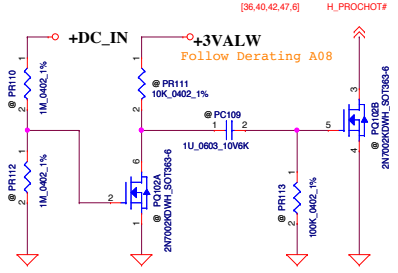




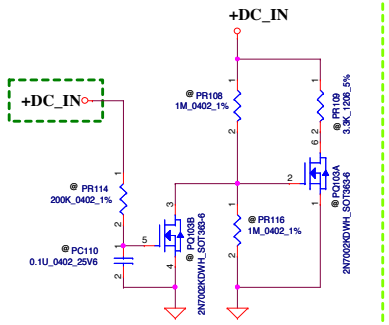
Other component(37.1)

Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

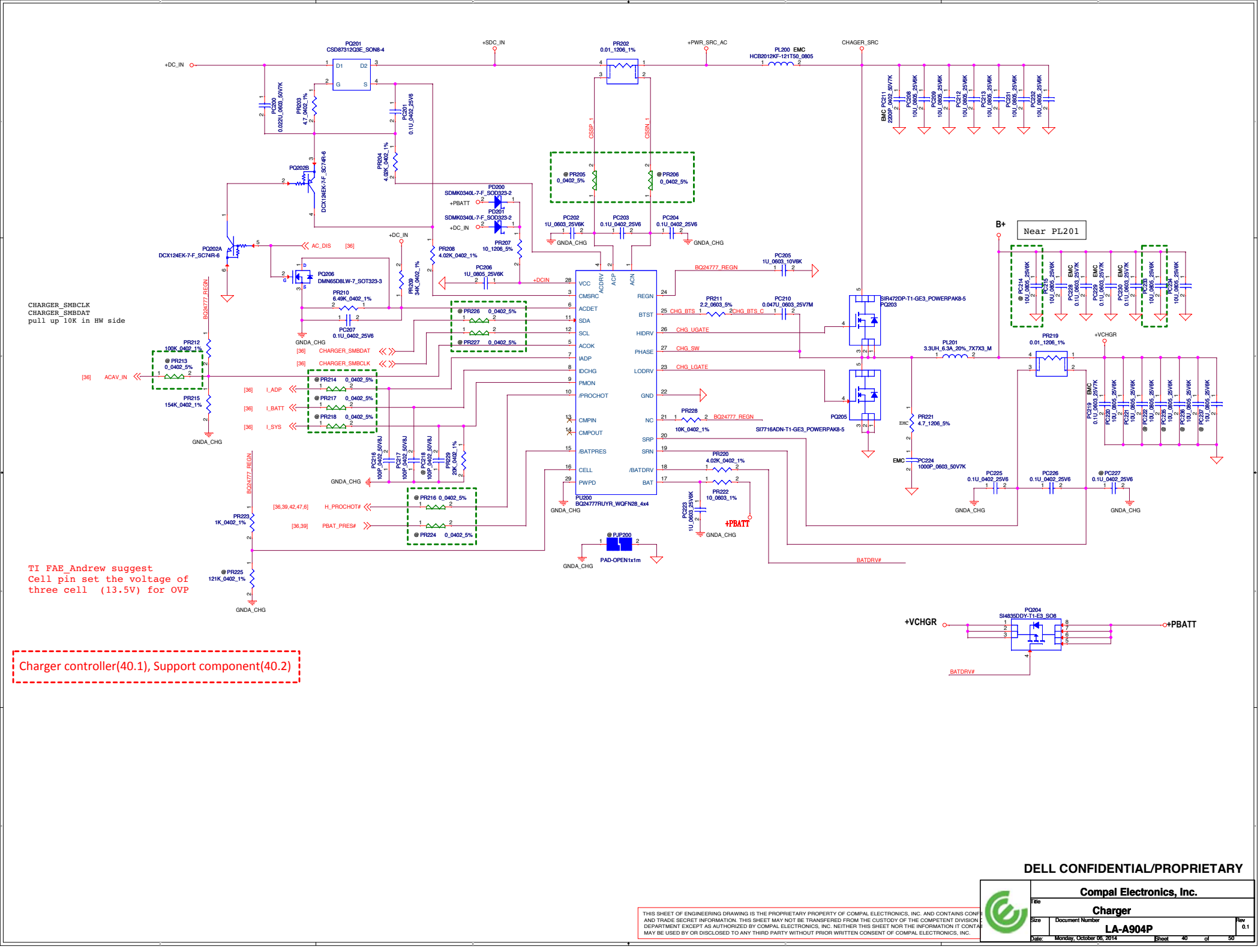
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

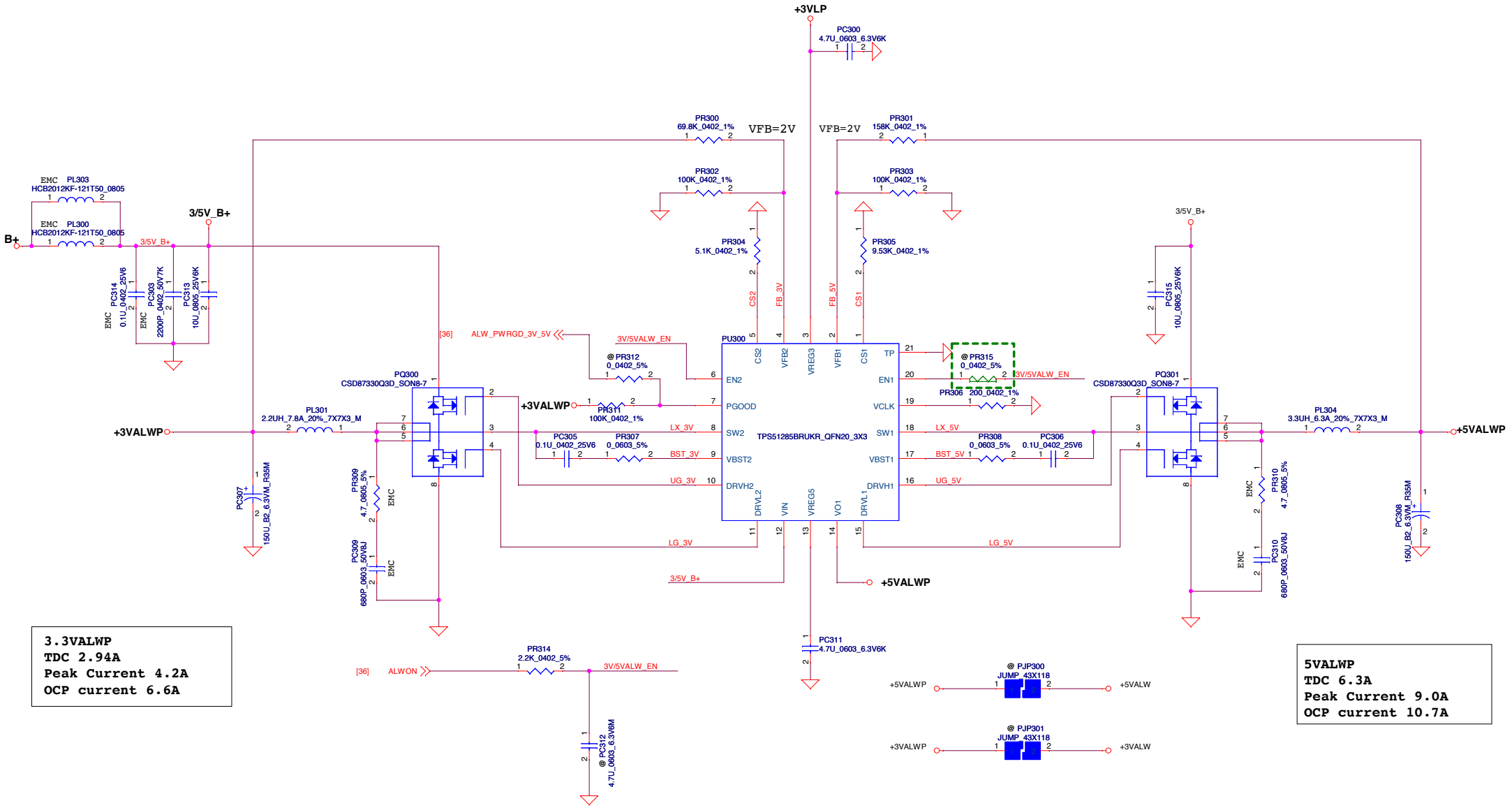
Compal Electronics, Inc.

Title: *PWR_DCIN/BATT CONN*

Size | Document Number: *LA-B072P* | Rev: 2.0

Date: Monday, October 06, 2014 | Sheet 39 of 50


CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side
TI FAE_Andrew suggest
Cell pin set the voltage of
three cell (13.5V) for OVP
Charger controller(40.1), Support component(40.2)
Near PL201
+DC_IN
+SDC_IN
+PWR_SRC_AC
CHAGER_SRC
+PBATT
+VCHGR
BATDRV#
GNDA_CHG
PU200 BQ24777RUYR_WQFN28_4x4
PAD-OPEN1x1m
SI7716ADN-T1-GE3_POWERPAK8-5
SIR472DP-T1-GE3_POWERPAK8-5
SI4835DDY-T1-E3_SO8
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
LA-A904P
Rev 0.1
Monday, October 06, 2014
Sheet 40 of 50



3.3VALWP
TDC 2.94A
Peak Current 4.2A
OCP current 6.6A

5VALWP
TDC 6.3A
Peak Current 9.0A
OCP current 10.7A

3V/5V controller(35.1), Support component(35.2)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

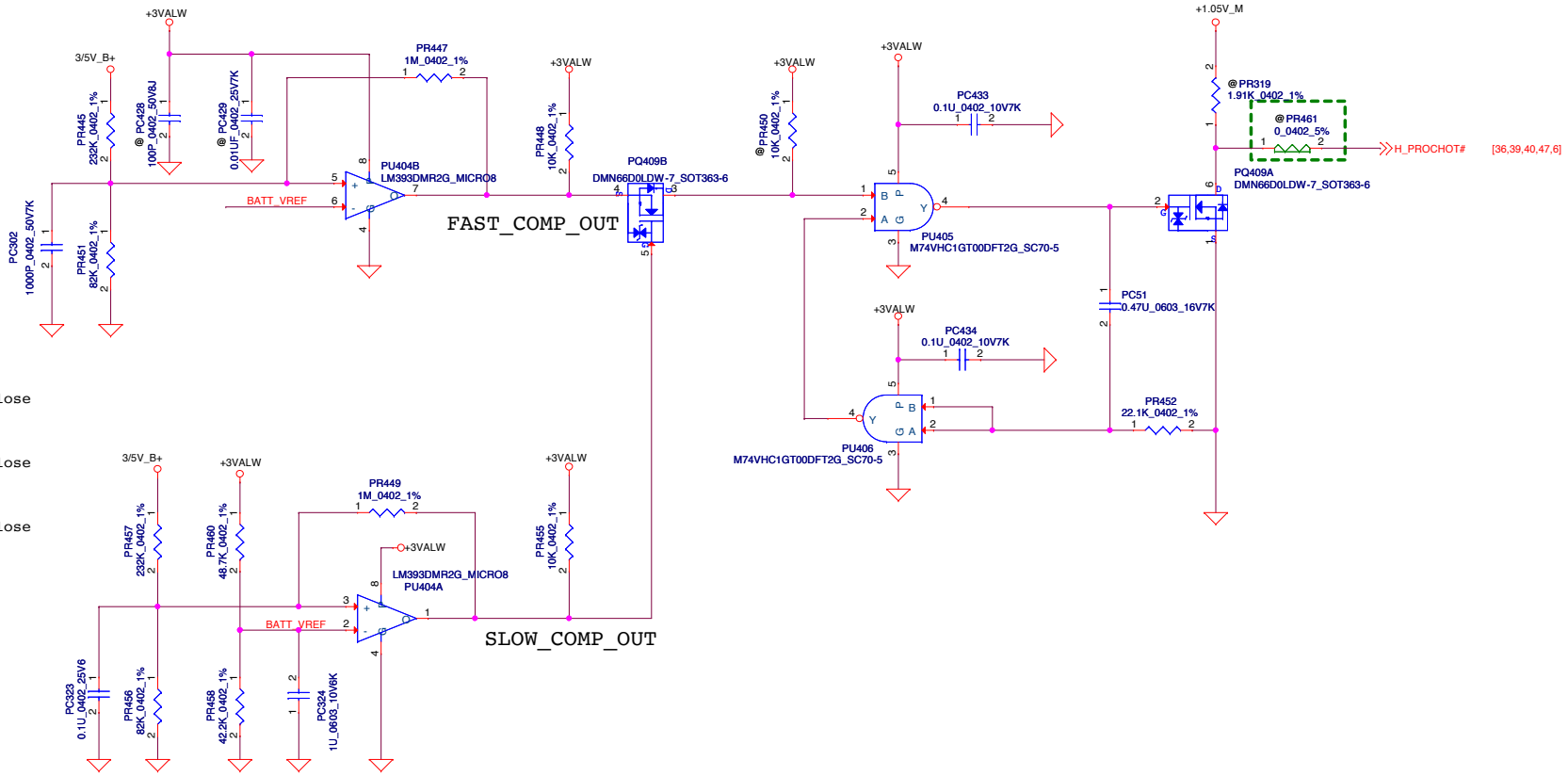
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P36-PWR_+3.3/5V_VR

Size: | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 41 of 50



PU404_Main source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.05V PA409A close

PU404_2nd_source
PQ409A open at 3/5V_B+ below 5.72V
and 3/5V_B+ recover 6.05V PA409A close

PU404_3rd_source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.04V PA409A close

Component(37.1)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
Title: P37-Blank		
Size	Document Number: LA-9261P	Rev: 0.1
Date: Monday, October 06, 2014	Sheet 42 of 50	

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

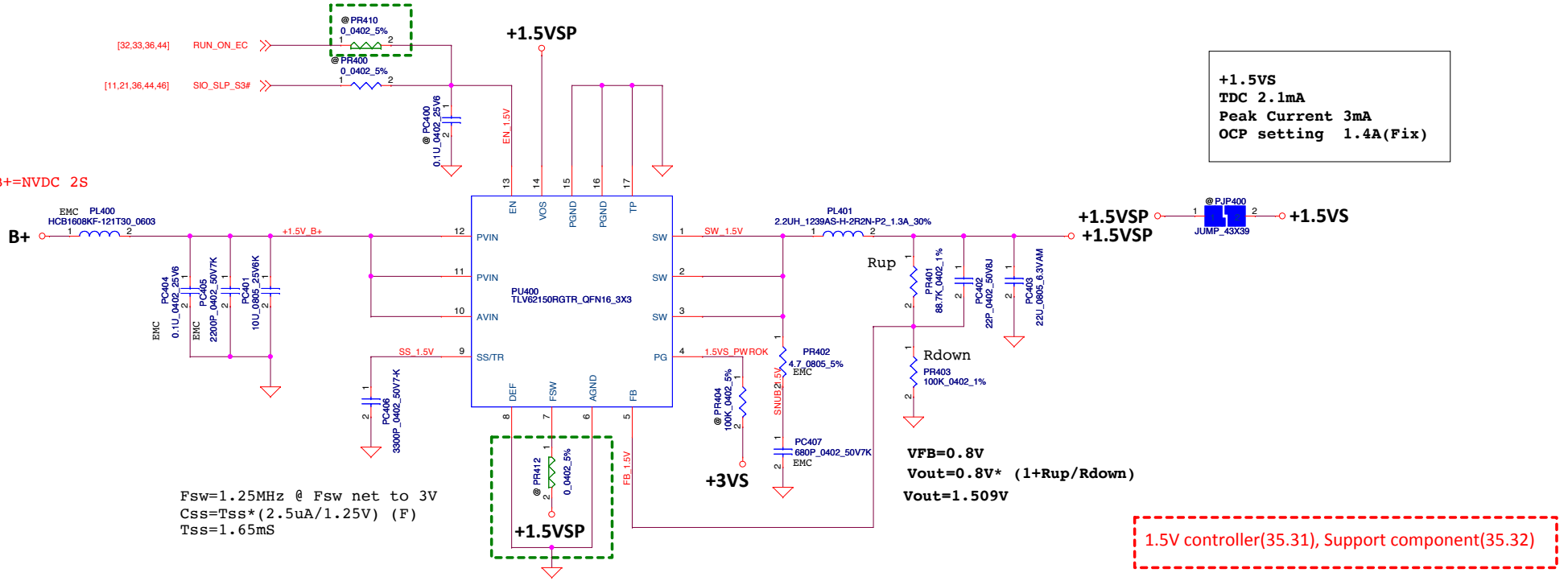
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **P38-Blank**

Size | Document Number: **LA-9261P** | Rev: 0.1

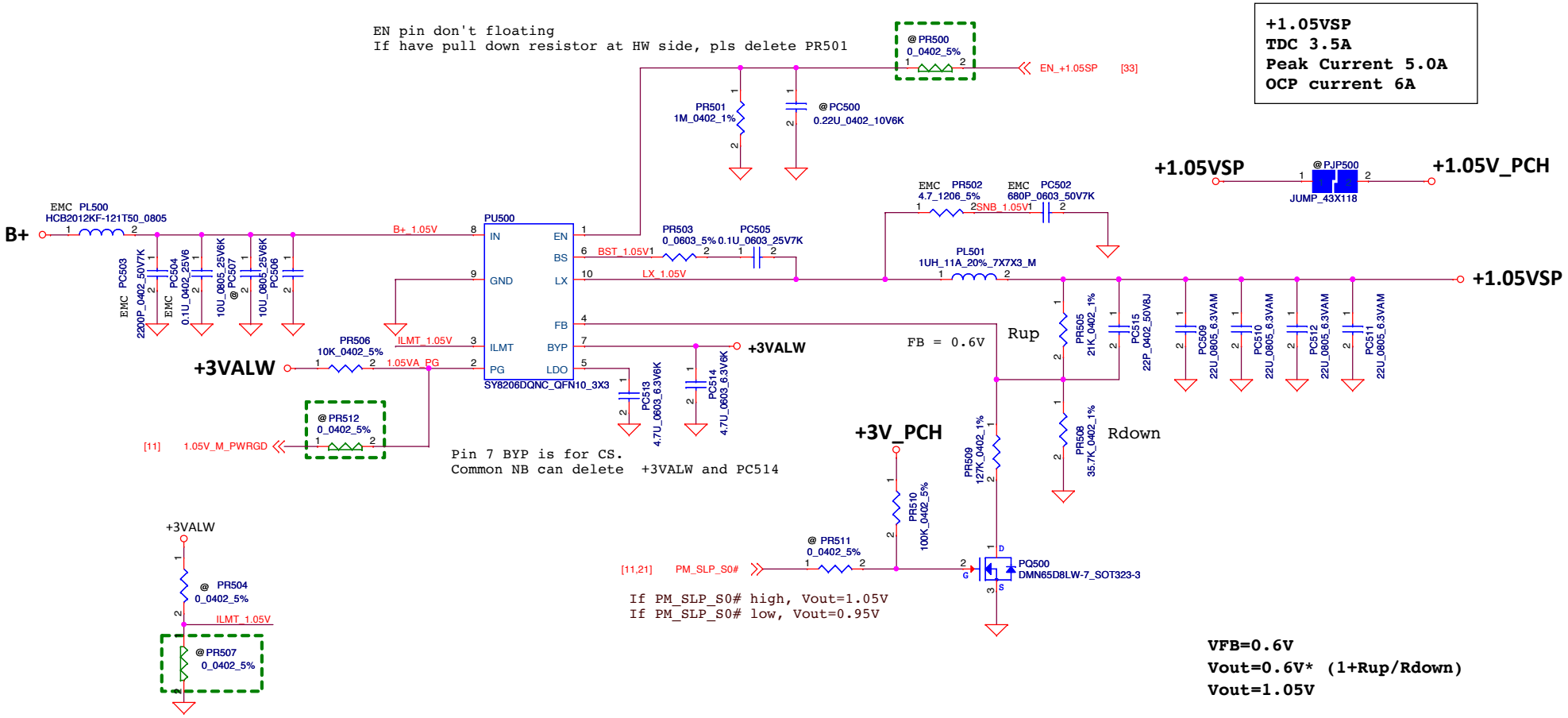
Date: Monday, October 06, 2014 | Sheet 43 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title	P39-PWR_+1.5VS/+1.8V_DDR		
Size	Document Number	LA-9261P	Rev 0.1
Date: Monday, October 06, 2014	Sheet 44 of 50		



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P40-PWR_+1.05VA

Size: A | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 45 of 50

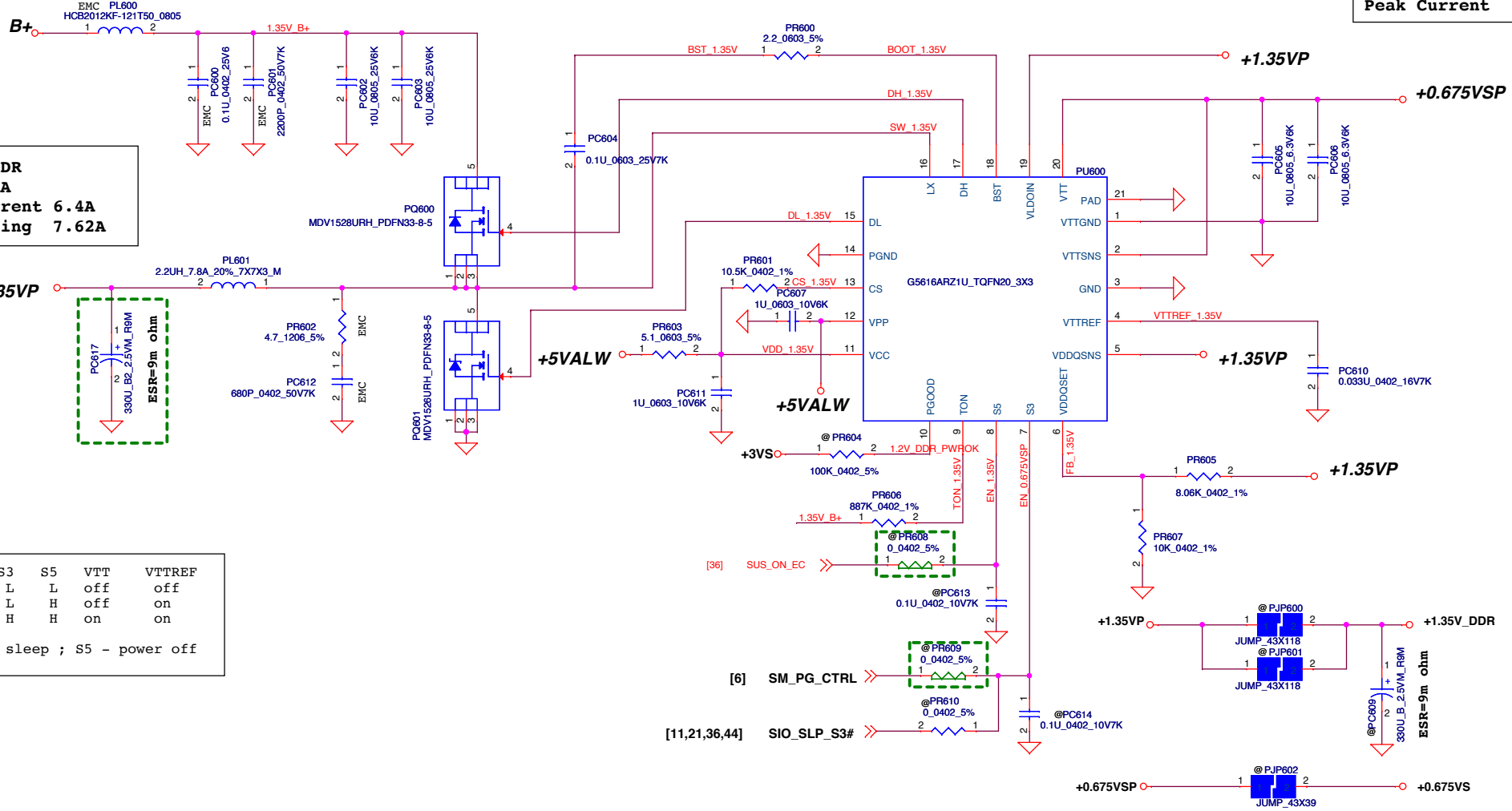
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35V_DDR.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

+1.35V_DDR
TDC 4.48A
Peak Current 6.4A
OCP setting 7.62A

Mode	S3	S5	VTT	VTTREF
Shutdown	L	L	off	off
Stadby	L	H	off	on
Normal	H	H	on	on

Note: S3 - sleep ; S5 - power off



DDR controller(35.3), Support component(35.4)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P41-PWR_+1.35V_DDR/+0.675VS

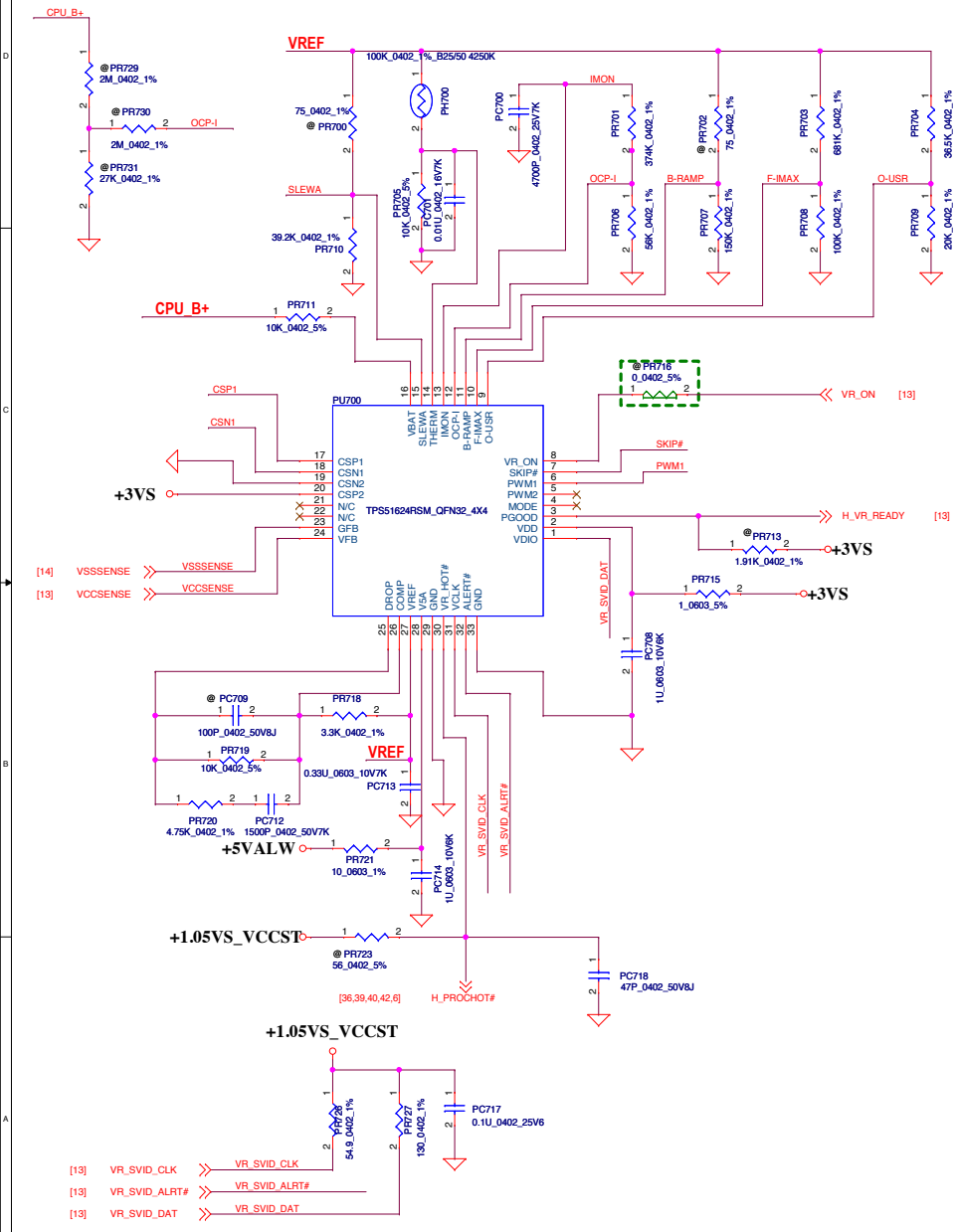
Size: | Document Number: LA-9261P | Rev: 0.1

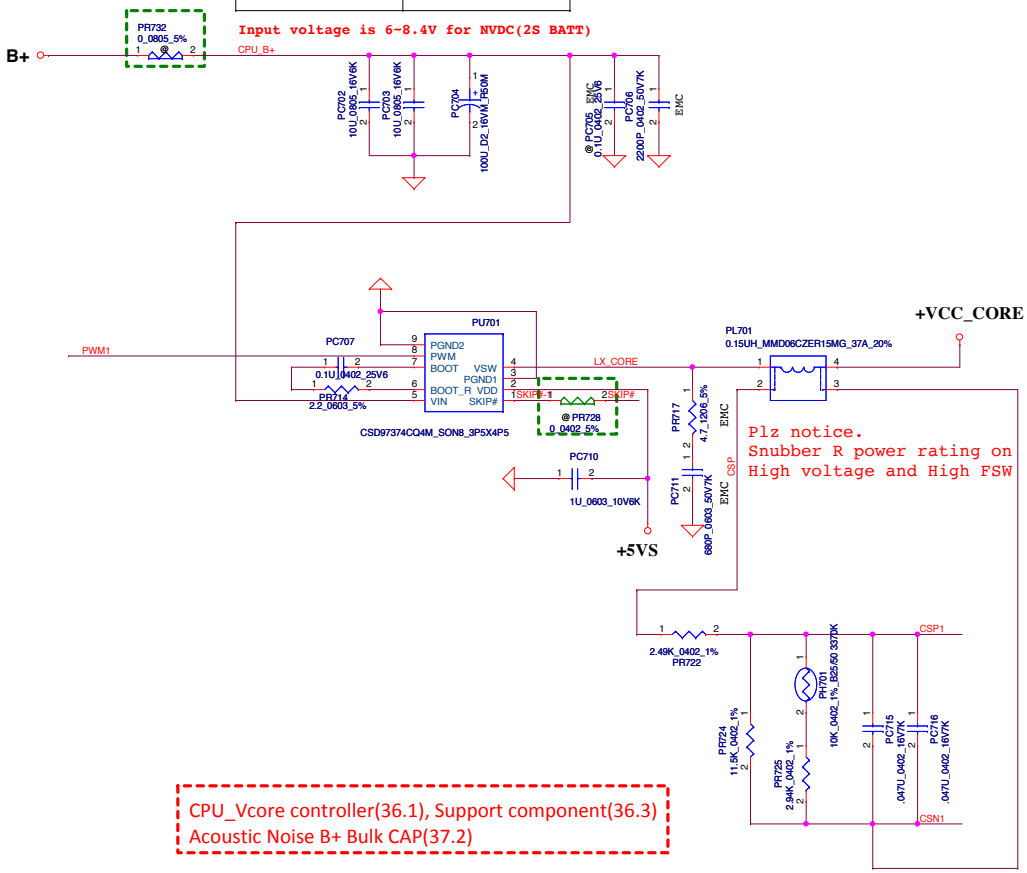
Date: Monday, October 06, 2014 | Sheet 46 of 50

Follow Intel 514849_514849_BDW_PDG_Rev_1.0

15W	Specifications
Vps0	1.8V
Vboot	1.7V
Icc_MAX	32A
Idyn_MAX	27A
Icc-TDC	10A
Load-Line	2.0mV/A
Fast Slew Rate	48mV/us

CPU
Frequency = 1.2MHz
PL2 Current 14A
ICC MAX 32A
OCP Current 39 A
IC_Dyn_VID1 27A
DCR: 0.9mohm +-7%
PH700 100Kohm B value: 3370k 1%
PH701 10Kohm B value: 4250k 1%





CPU_Vcore controller(36.1), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

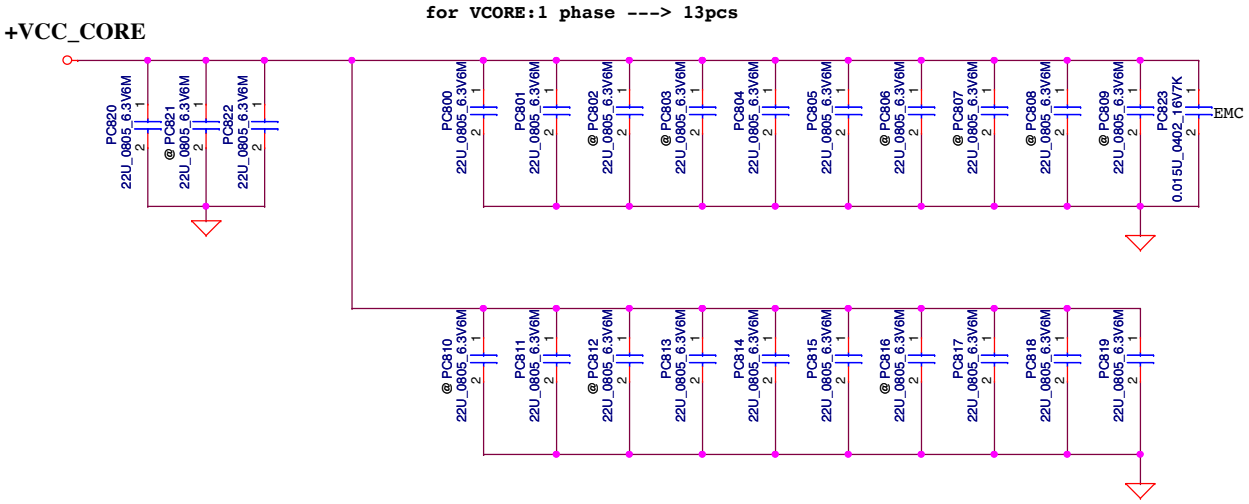
Compal Electronics, Inc.

Title: **P42-PWR_CPU_CORE**

Size: | Document Number: **LA-9261P** | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 47 of 50

CPU_Core output CAP(36.4)



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: P43-PWR_PROCESSOR_DECOUPLING

Size | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 48 of 50

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P40	PR205, PR206, PR213, PR214, PR216, PR217, PR218, PR224, PR226, PR227,	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
2	P41	PR315	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
3	P42	PR416	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
4	P44	PR410, PR411, PR412, PR413,	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
5	P45	PR500, PR507, PR512	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
6	P46	PR608, PR609	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	
7	P47	PR716, PR718, PR732	2014'10/06	Compal_Henry	modify schematic for A00 garber	Change 0 ohm to short pad	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P45-PWR_PIR-2

Size: C | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 49 of 50

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
				P44-PWR_PIR-1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: D, Document Number: LA-9261P, Rev: 0.1	
				Date: Monday, October 06, 2014	Sheet 50 of 50